UNCOMMITTED GaAs MMICs ASSEMBLED BY FLIP-CHIP SOLDER BONDING

F.J. Cotton, D.J. Warner, B.J. Buck, K.L. Pickering

ABSTRACT

A technique has been developed for the assembly of GaAs MMICs using flip-chip solder bonding. The additional process steps needed to permit solder bonding are compatible with fabrication in the Plessey GaAs MMIC Foundry. Flip-chip bonding allows reproducible, high integrity interconnections to be made in a single assembly operation, while adding the design freedom of mid-chip connections. The key to the success of the technology is the provision of a barrier metallisation layer interposed between the solder and the gold bond pads of the MMIC and MIC substrate circuitry.

Demonstrator receiver MMICs were designed, fabricated, assembled and tested. The GaAs chip was designed as unconnected building block circuits and the receiver function generated by interconnection tracks on the MIC substrate. Clearly different microwave operating parameters were derived from the same GaAs chip design by altering the MIC design. Selective receiver operation was demonstrated between 2 and 7 GHz, with up to 20 dB conversion gain.

INTRODUCTION

The low quantity, specialised microwave circuit requirements of many systems applications make the design of dedicated, wholly integrated GaAs MMICs potentially expensive. In addition, circuit design iterations tend to be time-consuming and involve considerable further expense. The design approach presented here represents a possible low cost solution to this difficulty. Final circuit function was generated by the interconnection tracks on a microstrip substrate, which connected together GaAs sub-circuits by means of flip-chip solder bonding. The MMIC sub-circuits were designed on a single GaAs chip as unconnected functional blocks. Altering the design of the microstrip circuit allowed some or all of the available sub-circuits to be accessed, thereby generating alternative microwave performances from the same GaAs chip design.

SOLDER BONDING TECHNOLOGY

Gallium arsenide MMICs are generally designed with bond pads at the chip periphery in order to simplify the process of wire or tape bonding. Where interconnections are required within the body of the chip, the standard process provides through-chip vias for ground connection, but wire bonding to the centre of the chip is inadvisable from yield and reliability considerations and adds considerable parasitic inductance for RF connections. Flip-chip bonding surmounts these difficulties while giving the further advantage of allowing all interconnections to be made in a single assembly operation. Flip-chip bonding of discrete GaAs FETs has been employed for many years [1-3], but GaAs MMICs to date have been wire bonded. The technique used here was that of controlled solder reflow under surface tension forces [4], modified to take account of the gold-based metallisations conventionally used in MMICs.

Metallurgical interactions between gold and tin-lead solders would normally render this type of solder unsuitable for flip-chip bonding GaAs devices. However, the range of melting points available and in particular the relatively high liquidus temperature of 95 wt.% lead:5% tin (310°C), make these solders very attractive. The 95:5 composition is of interest since subsequent assembly operations, such as die attach, chip resistor attach or thermosonic wire bonding, may be carried out at temperatures as high as 250°C without disruption of the original flip-chip bonds. In order to be able to employ tin-lead solders, it was therefore necessary to provide a metallurgical barrier between the solder and the gold-based bond pads on the circuitry [5].

The authors are with Plessey Research Caswell Limited, Allen Clark Research Centre, Caswell, Towcester, Northants., England.

Cross-sections of the structure of the bond prior to flip-chipping are shown in Figure 1. For convenience of fabrication, solder was deposited on the ceramic half of the hybrid, but the solder could equally well be defined on the MMIC. The barrier metallisation described above was a thin layer of either sputtered chromium or titanium, which both have the additional property of not being wetted by molten solder.

The barrier metal was patterned either by ion beam milling or by wet chemical etching. Within the area of non-wettable barrier metal, a further solder-wettable metal layer was defined by lift-off. This film was formed of sequential layers of chromium, chromium-copper, copper and gold. The initial chromium layer provided adhesion to the underlying barrier metal, while the remaining metals gave good solderability to tin-lead. The evaporated solder de-wets from the barrier metal when raised above 310°C, forming truncated spheres on the circular wettable metal areas.

Flip-chip solder bonded device assemblies were generated by aligning the two components and reheating above 310°C. Surface tension forces acted to self-align the MMIC to the ceramic circuitry as the solder bond formed. Alignment accuracies within two microns were observed.

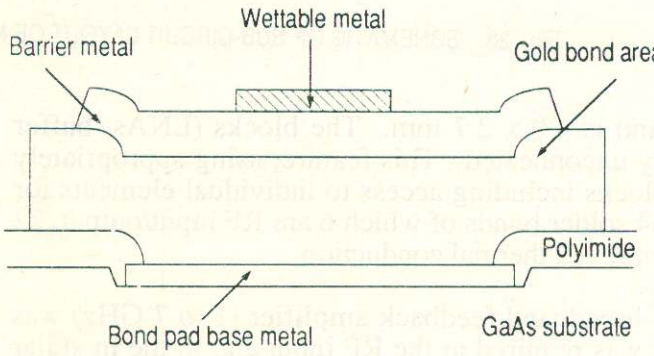

Fig. 1a. SOLDER BOND STRUCTURE ON GaAs MMIC

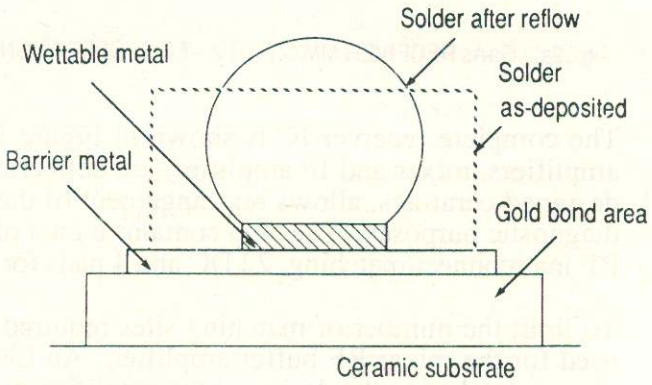

Fig. 1b. SOLDER BOND STRUCTURE ON CERAMIC SUBSTRATE

CIRCUIT DESIGN AND FABRICATION

Active and passive GaAs test components when flip-chip bonded have been shown to behave in very similar fashion at microwave frequencies to their wire-bonded equivalents [6]. Small signal S-parameters are little affected by the method of chip mounting. Flip-chip bonding was found to reduce the spread in device characteristics across a wafer, since the flip-chip bond is more reproducible than wire bonds. It was therefore possible to design test circuits using the existing Plessey Foundry component database. Furthermore, since the additional steps needed to generate the solderable bond pads are entirely compatible with the Foundry process, the standard fabrication sequence was employed to produce demonstrator MMICs.

The design and test of an uncommitted receiver chip to operate in S- and C-bands was chosen as a suitable demonstrator of the power of the flip-chip technology. A variety of microstrip ceramic designs was to be provided to access a single GaAs chip design. The ceramic variants were to be such that the GaAs chip could be demonstrated in operation at two distinct frequencies, determined by the microstrip circuitry:

Frequency range	S-band minimum
Conversion gain	15-20 dB
LO power	-10 dBm
Noise figure	3 dB
IF range	DC to >500 MHz
Input/output impedance	100 ohm balanced

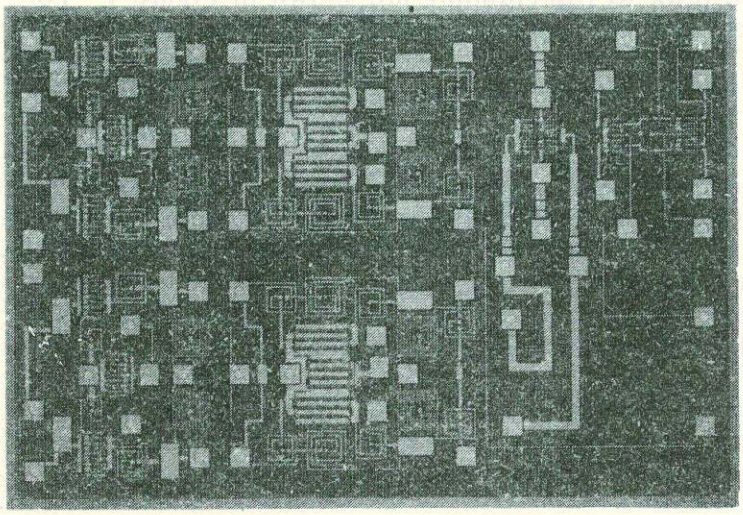

Fig. 2a. GaAs RECEIVER MMIC FOR 2 - 7 GHz OPERATION

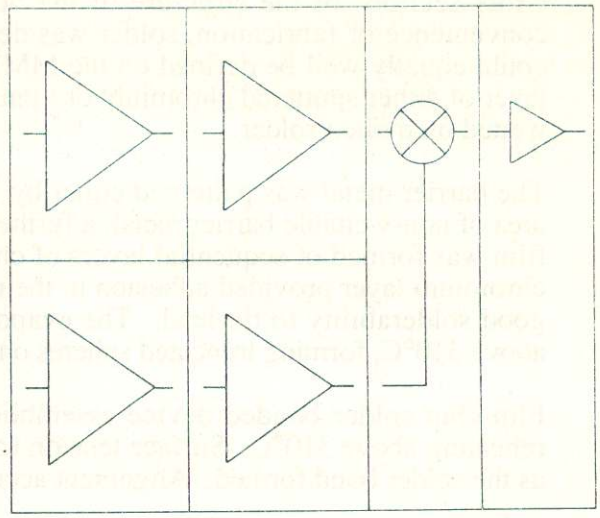

Fig. 2b. SCHEMATIC OF SUB-CIRCUIT LAYOUT OF MMIC

The complete receiver IC is shown in Figure 2 and is 4.0 x 2.7 mm. The blocks (LNAs, buffer amplifiers, mixer and IF amplifier) are deliberately unconnected. This feature, using appropriately designed ceramics, allows rearrangement of the blocks including access to individual elements for diagnostic purposes. The chip contains a total of 54 solder bonds of which 6 are RF input/output, 22 RF interconnect/matching, 22 DC and 4 pads for improved thermal conduction.

To limit the number of matching sites required, a broadband feedback amplifier (1 to 7 GHz) was used for the mixer RF buffer amplifier. An LNA was required at the RF input and in the modular approach taken to the design of the amplifier stages it was convenient to use an identical stage at the LO input. The mixer comprised an anti-parallel diode ring. Provision was made for a DC bias current to be applied through high value resistors. Diode RF impedance was calculated to be approximately 50 ohms + 1 pF for the "single-ended" parallel diode pair seen by each buffer amplifier.

RF/LO Mixer Buffer Amplifier

A single-ended feedback amplifier with approximately 7 dB gain over 1 to 7 GHz was used for the buffer amplifier. It was necessary to provide a series capacitor between amplifier and mixer presenting a high impedance compared with the mixer IF impedance, say 200 ohms, while presenting a low impedance compared with the RFA output impedance (50 ohms nominal). Attempting to satisfy both criteria with RFs to below 2 GHz and IFs to above 500 MHz required a capacitor of approximately 1.5 pF. Having chosen the blocking capacitor, the buffer amplifier output impedance must be conjugately matched to the diode plus blocking capacitor impedance. This was achieved with a single transmission line connected between the balanced outputs. Although in balanced operation the circuit will not be sensitive to the impedance at the virtual earth junction of the two FET sources, a high impedance current source was included. This improved the common mode rejection ratio (CMRR) of the amplifier which reduces the effect of any imbalance in the preceding stage(s). All DC bias points were common to both sides of the balanced amplifier, and being applied at virtual earth points removed the need for decoupling components.

Low Noise Pre-Amplifier

The low noise pre-amplifier design included source-peaking, series inductive feedback to permit minimum noise figure and minimum input reflection coefficient at the expense of a small amount of gain. With these input amplifiers, there is more freedom for the off-chip matching and both series and shunt transmission line matching were employed. Again, a long-tailed pair was used to investigate the possibility of using the chip with a single-ended LO.

IF Amplifier

The IF amplifier was designed to give minimum loading to the mixer at RF (input impedance greater than 1 kohm shunted by 0.1 pF), while providing approximately unity voltage gain from the relatively high IF impedance of the mixer to the external 50 ohms. The first stage was common source with small 150μm FETs for low input capacitance and the second stage was common drain to provide the output match. The interstage shunt capacitor was present for further roll off at RF and the long-tailed input pair rejected common mode LO from any imbalance in the diodes.

Ceramic Design

Off-chip ceramic circuitry was designed for the receiver MMICs, designed for alumina substrates. Two substrates were designed for operation at 3 and 6 GHz nominal, and a further two substrates had input connection direct to the buffer amplifier (bypassing the LNA) in order that the input and mixer tuning may be deconvolved.

The four variants are shown in Figure 3. A 12 x 12 x 0.254 mm substrate was chosen for compatibility with the microwave common module (MCM) format [7]. The RF and LO channels are symmetrical and connected to opposite edges of the ceramic. The DC connections for the RF and LO channels are brought to a third side, while mixer bias and IF amplifier DC supplies and the IF output are taken to the remaining edge. Care was taken to maintain the symmetry of the balanced inputs, the 3 GHz, LNA bypassed version requiring transmission line meanders.

The completed flip-chip assembly is shown in Figure 4. (Note that many of the DC connections are to common supply voltages and could have been interconnected locally to the IC. This design brings all of the bias lines out independently for diagnostic purposes).

MEASUREMENT RESULTS

After some preliminary measurements to confirm the mixing action of the flip-chip receiver assemblies, an automated test bench was set up to enable detailed measurements while varying a large number of operating parameters. A micro-computer was used to program RF and LO frequencies and power levels, and record IF output from the receiver under test via a spectrum analyser. The software allowed for one of five parameters - LO frequency, IF frequency, LO power, RF power and mixer bias voltage - to be swept and another parameter to be stepped during each measurement.

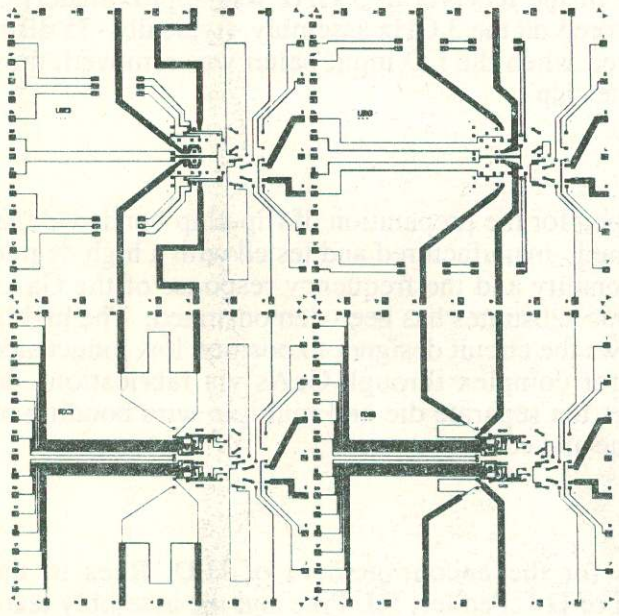

Fig. 3. RECEIVER CERAMIC SUBSTRATE DESIGNS

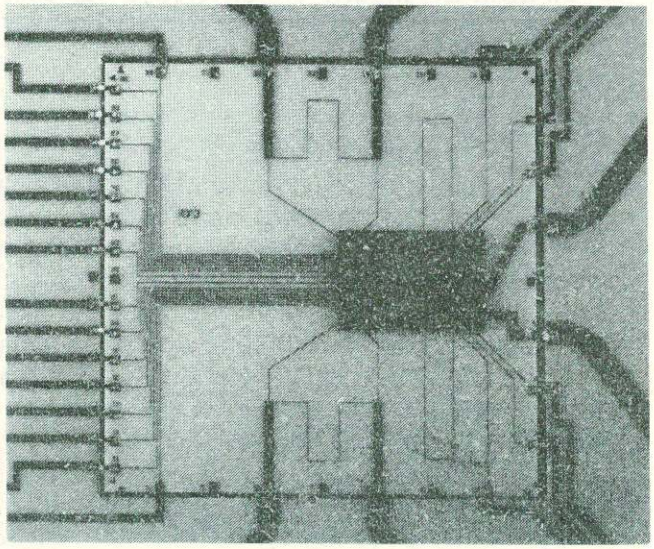

Fig. 4. FLIP-CHIP ASSEMBLY (3 GHz OPERATION)

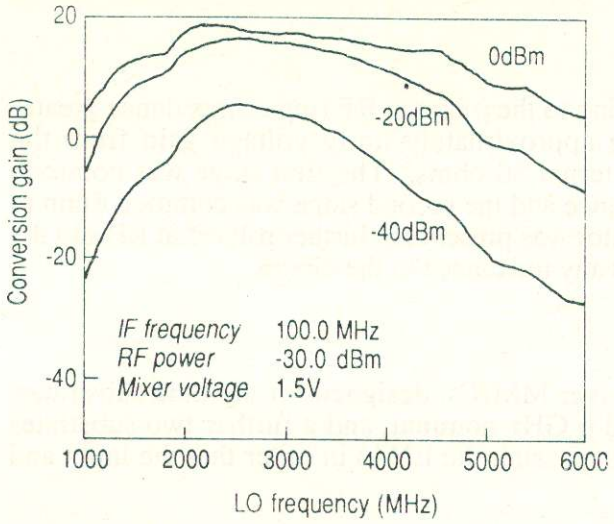

Fig. 5. CONVERSION GAIN FOR 3GHz CIRCUIT AS A FUNCTION OF LO POWER

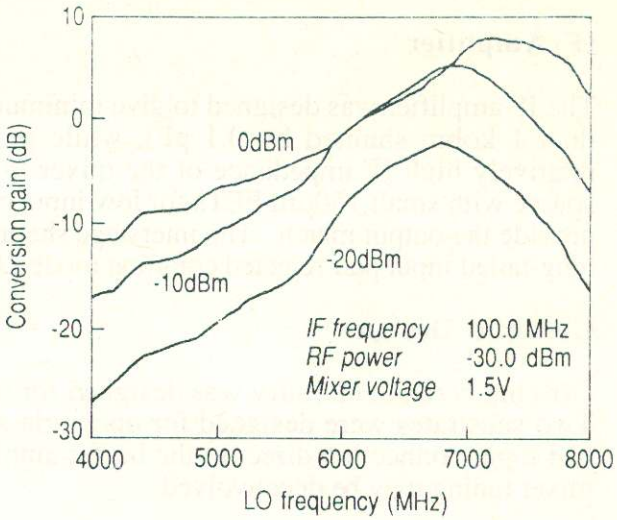

Fig. 6. CONVERSION GAIN FOR 7 GHz CIRCUIT (WITHOUT LOW NOISE AMPLIFIER SUB-CIRCUITS) AS A FUNCTION OF LO POWER

A sample measurement for the 3 GHz receiver assembly is shown in Figure 5. Satisfactory operation is indicated with conversion gains in excess of 15 dB with moderate selectivity for LO powers of -20 to -10 dBm. Comparing the frequency response with that from the 3 GHz assembly in which the LNA was bypassed, we observed a change of centre frequency from just over 3 GHz to 2.6 GHz, possibly indicating some mis-alignment of the input matching with the tuned mixer response. If the two responses had better coincidence, we could expect greater selectivity. The IF response indicated conversion gain falling to 0 dB at about 1.5 GHz.

The response for the nominal 6 GHz tuned assembly with bypassed LNA is shown in Figure 6. The centre of the tuned response was slightly high in frequency: 6.8 GHz at low LO drive and increasing to nearly 7.5 GHz at significant drive levels. This frequency is beyond the intended range of operation for the buffer amplifier, but nevertheless conversion gains of up to 8 dB were obtained.

Measurement of noise figure was made difficult due to the unscreened nature of the mixer test fixture, but it was established that the overall noise figure of the receiver at 3 GHz was approximately 3 dB.The LO breakthrough at the IF output was monitored on the 3 GHz assembly (typically -35 dBm for -20 dBm LO input). No difference was observed when the LO input balun was removed, thus demonstrating the common mode rejection ratio of the chip.

CONCLUSIONS

A Foundry-compatible technology has been developed for the preparation of flip-chip bonded GaAs MMICs. A multi-function GaAs MMIC was designed, manufactured and tested with a high degree of success. The ability to modify both the functionality and the frequency response of the GaAs MMIC by flip-chip solder bonding to specific ceramic substrates has been demonstrated. The highly reproducible nature of the flip-chip solder bond allows the circuit designer to position low inductance bonds anywhere in the MMIC without the need for complex through-GaAs via fabrication. In addition, a single solder bonding operation replaces the separate die and multiple wire bonding of conventional MMICs, greatly reducing assembly time and costs.

ACKNOWLEDGEMENTS

The authors would like to express their thanks for the encouragement of H.D. Rees in the development of the uncommitted MMIC. The help of D.J. Pedder, S.J. Pike and the assembly team led oy J.A. Sparrow is also gratefully acknowledged. This work has been supported and sponsored by the Procurement Executive, Ministry of Defence (Royal Signals and Radar Establishment).

REFERENCES

[1] S. Bharj, H. Balshem, "Ku-band power FET amplifiers use flip-chip FET devices" Microwave System News, 15, 8, 75-80 (1985).

[2] R.L. Camisa, G. Taylor, W. Reichert, F. Cuomo, R. Brown, "A flip-chip GaAs power FET with gate and drain via connections", IEEE Electron Device Letters, EDL-5, 4, 118-120 (1984).

[3] G.C. Taylor, M. Eron, D.W. Bechtle, S-G. Liu, R.L. Camisa, "High efficiency 35 GHz GaAs MESFETs', IEEE Trans. Electron Devices, ED-34, 6, 1259-1263 (1987).

[4] L.S. Goldmann, P.A. Totta, "Area array solder interconnections for VLSI", Solid State Tech., 26, 6, 91-97 (1983).

[5] Patents Pending.

[6] D.J. Warner, K.L. Pickering, D.J. Pedder, B.J. Buck, S.J. Pike, "Flip chip-bonded GaAs MMICs compatible with Foundry manufacture", to be published.

[7] D.S. James, W.F. Winder, I.M.H. Williamson, K.R. Harris, S.W. Redfern, D.A. Williams, M.S. Peters, B. Mazonas, "Microwave common modules", IEE Colloquium on Manufacturing and Integration Techniques for Microwave Circuits, Digest 1988/102, October 1988.