STATE OF THE ART GaAs PIN AND FET MONOLITHIC SWITCHES

L. Raffaelli, G. Dawe, D.C. Bartle, D. Payne, S. Bandla*

Abstract

Switching and routing of RF signals are very common function in EW, radar and communications system.

This paper describes the design, fabrication and performance of state of the art Broadband MMIC Switches based on MESFET and PIN Diode Devices.

FET SWITCH DEVICE DESIGN

The GaAs MESFET [1] has gained wide spread popularity as an RF switching device. Excellent performance has been achieved past 20 GHz. When a FET is used as a switch, the gate terminal, which is naturally decoupled from the source and drain terminals is used as the control port. The channel region between source and drain is switched between a high impedance (fully depleted of carriers, off state) and a low impedance, (small bulk resistance, on state).

The design parameters of the FET switch are "on" resistance Ron and "off" state resistance Roff and off state capacitance Coff. These device parameters directly effect switch performance in the areas of insertion loss, isolation and switching speed.

An increase in the doping density of the active layer of the device will lower Ron but will increase Coff because of increases in Cdg and Cgs. An increase in thickness of the active layer also will decrease Ron and increase Coff.

In order to minimize both of these parameters simultaneously, .25um gate length FETs were used. Most of the FET switches reported to date [2] employ 1 or .5um gate length FETs. The .25um MESFET has a reduced source to drain spacing which leads to a lower Ron. Coff is slightly reduced because of the small gate dimension.

Direct ion implantation into (100) semi-insulating LEC GaAs substrates and rapid thermal annealing provide active layers for the FET switch. A surface N+ layer was implanted to reduce ohmic contact resistance and minimize source to gate and drain to gate resistance of the gate recessed MESFET structure. A deeper channel layer with

*The authors are with Alpha Industries, Woburn, MA.

free electron concentration of 4 x 10^{17} cm^{-3} was provided by a second $^{29}Si^{+}$ implant.

FET SWITCH FABRICATION

Active layer device areas and GaAs resistors were defined and electrically isolated from each other by shallow mesa etching. AuGe/Ni/Au ohmic contacts were produced by evaporation and lift off followed by a 465°C alloy. Sputter deposition and lift off was employed to produce 20 ohm Ta resistors. The 0.25um gates were electron beam direct written in PMMA and gate recess etching performed prior to evaporation of gate metal. After gate metal lift off, transmission lines and D.C. bias pads were also defined by evaporation and lift off. A passivation/protection layer on the MESFET channel areas was provided by 1500A of PECVD Si_3N_4 and RIE. Metallization and plating on the back of the wafer provided a ground plane and through via grounding. Street etching and chip separation were the final steps of the process.

FET SWITCH CIRCUIT DESIGN

The basic arm (1.8 x 1.2mm) consists of a series FET and three shunt FETs (see Fig. 1). The series FET allow switching operation to D.C. The shunt FETs periodically load the output transmission lines at distances that optimize VSWR and isolation. The small gate periphery of the series device and consequently the small Coff aides in maintaining high isolation at 20 GHz. The shunt FETs have larger gate widths for low Ron which improves isolation.

In the non reflective configuration additional series and shunt FETs plus a Ta resistor are added to the output to maintain low VSWR in the off state.

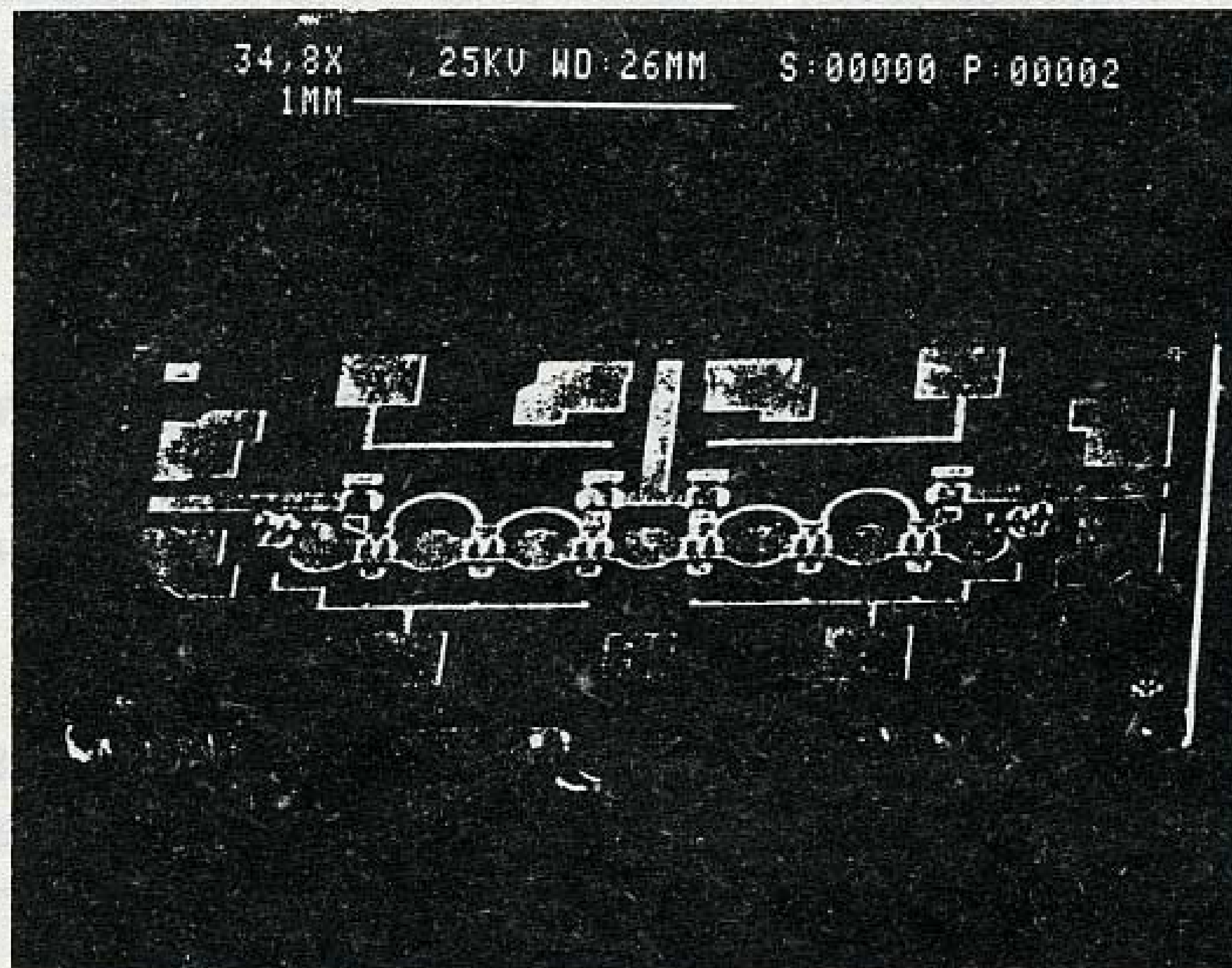


FIGURE 1. SPDT FET SWITCH

PIN SWITCH DEVICE DESIGN

For a fully depleted intrinsic layer the reverse biased capacitance is determined by the diode cross sectional area and the intrinsic layer thickness. The forward biased resistance has components due to the P and N terminals and a current dependent resistance of the intrinsic layer. Resistance due to P and N terminals is minimized by diode design, and the use of highly conductive active layers of optimum thickness. For a given forward bias current the intrinsic layer resistance is determined by the layer thickness and the injected carrier lifetimes and mobilities. Long carrier lifetimes and high mobilities are required for low resistance and are dependent on the material growth technology. The intrinsic layer thickness must be chosen to satisfy both resistance and capacitance of the diode.

The PIN structures were grown by MOCVD on LEC semi-insulating GaAs substrates. The top P-type layer was 0.4um thick with a free hole concentration of 2×10^{19} cm^{-3}. The middle 5×10^{14} cm^{-3} n-type intrinsic layer was 3um thick and a 4um thick 2×10^{18} cm^{-3} N+ layer was grown on the semi-insulating substrate.

Fig. 2 is a photograph of the double mesa PIN diode structure. The inner mesa defines the diode area and the outer mesa provides inter device electrical isolation and defines the N+ terminal. Air bridge connections are made to the P+ terminal while transmission lines up the side of the outer mesa connect to the N+ terminal.

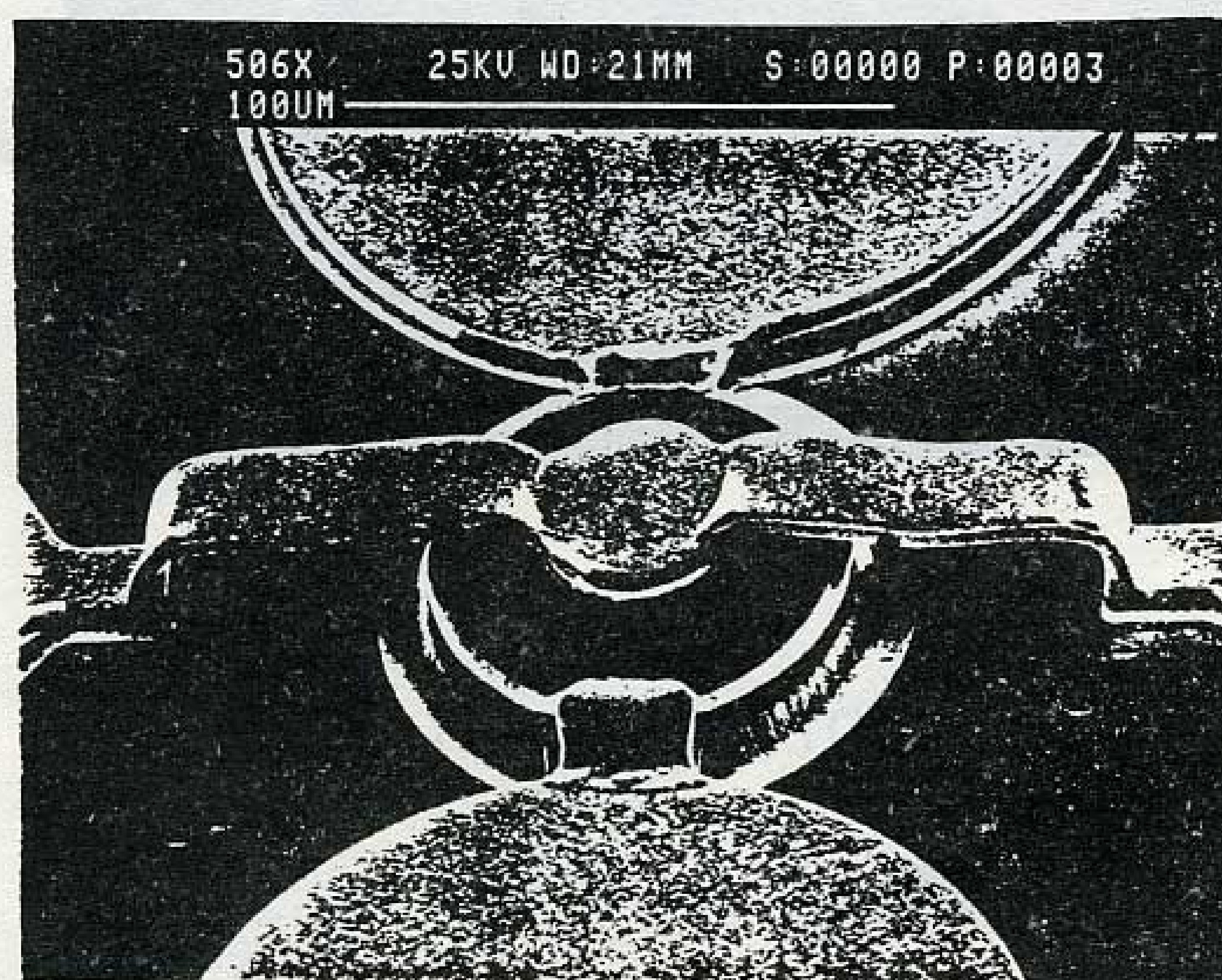


FIGURE 2. MONOLITHIC PIN DIODE

PIN SWITCH FABRICATION

The circular double mesa structure, illustrated in Fig. 2, was produced by isotropic etching. Au/Ag/Zn and Au Ge/Ni/Au evaporated films were alloyed into the P+ and N+ terminals respectively to form ohmic contacts. With the PIN diodes defined, fabrication of the monolithic circuit follows a similar sequence described earlier in the FET switch section.

SPDT PIN SWITCH CIRCUIT DESIGN

For high isolation and broadband coverage a series shunt, shunt configuration was used. The layout is shown in fig. 3. The length of the transmission line between the two shunt diodes has been optimized to provide high isolation in the "off" state and low insertion loss in the "on" state. DC blocking capacitors are provided in each area and bias to the series and shunt diodes is applied through external choke. The chip size is 3.5 x 1.5 mm.

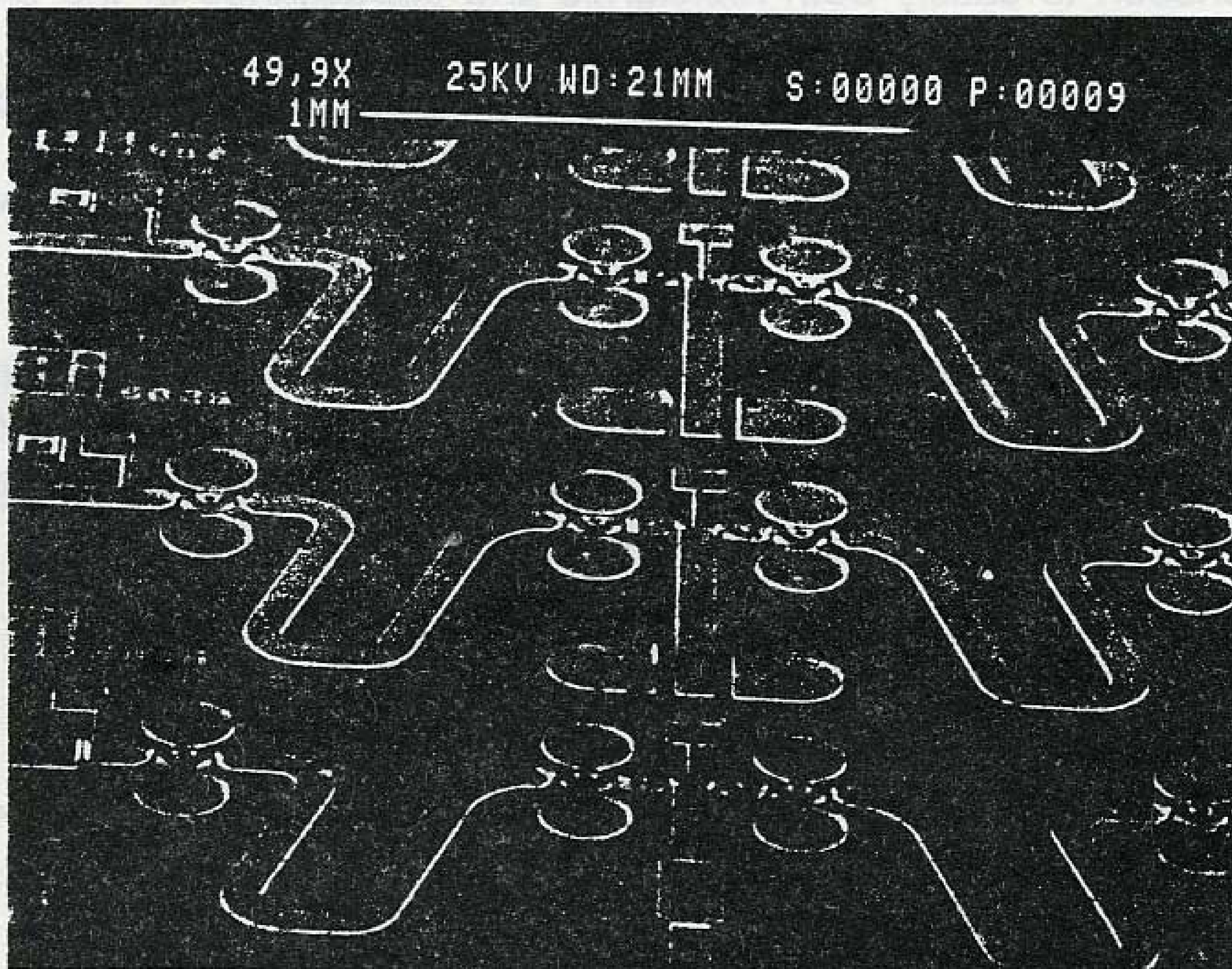
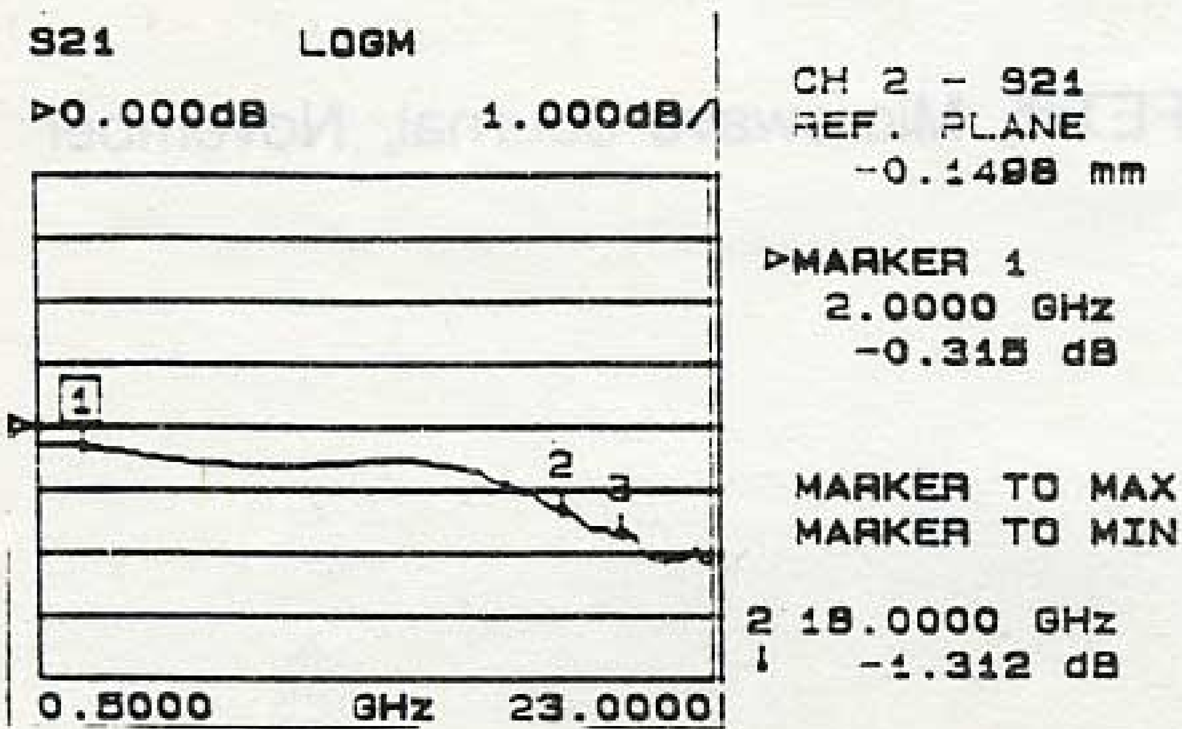


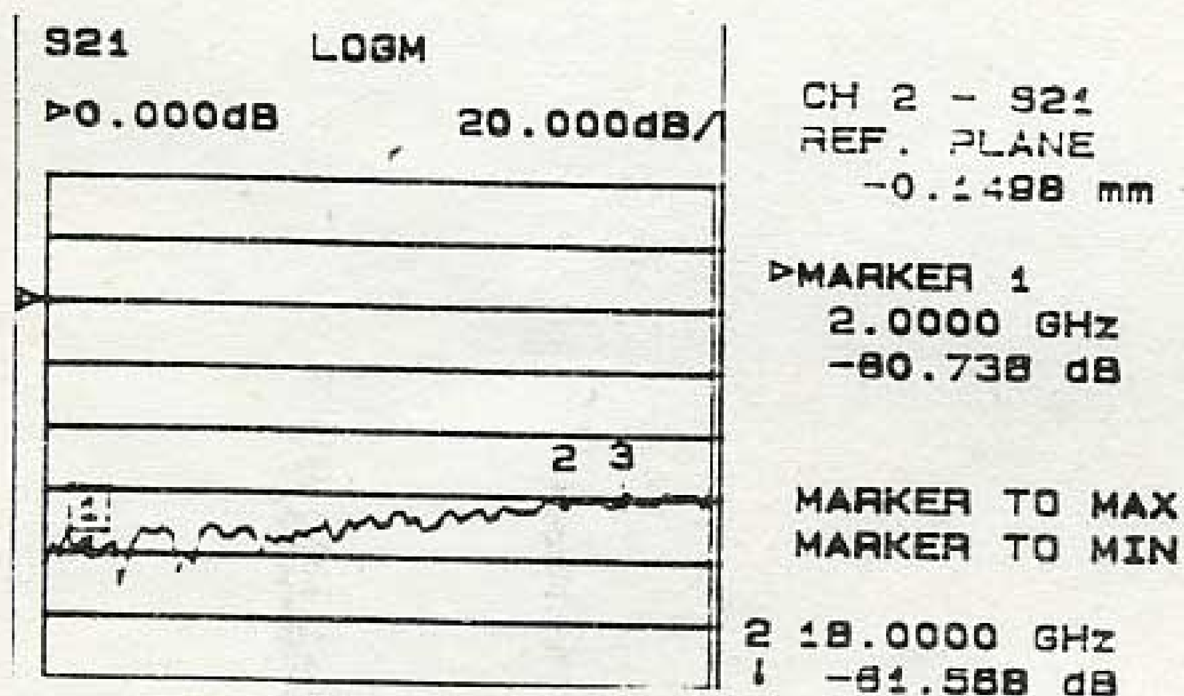
FIGURE 3. SPDT PIN SWITCH

TEST RESULT

The SPDT non reflective FET switch provided less than 2dB insertion loss and a minimum of 55dB isolation up to 18 GHz (see Fig. 4). The SPDT PIN Switch demonstrated a minimum of 60dB isolation and 1.5dB insertion loss up to 18 GHz (see Fig. 5). The return loss was better than 10dB for both types of switches. The switching speed of the FET and PIN Switches was less than 1ns and 2ns respectively between 10 and 90%. We believe these to be state of the art results for MMIC Switches.

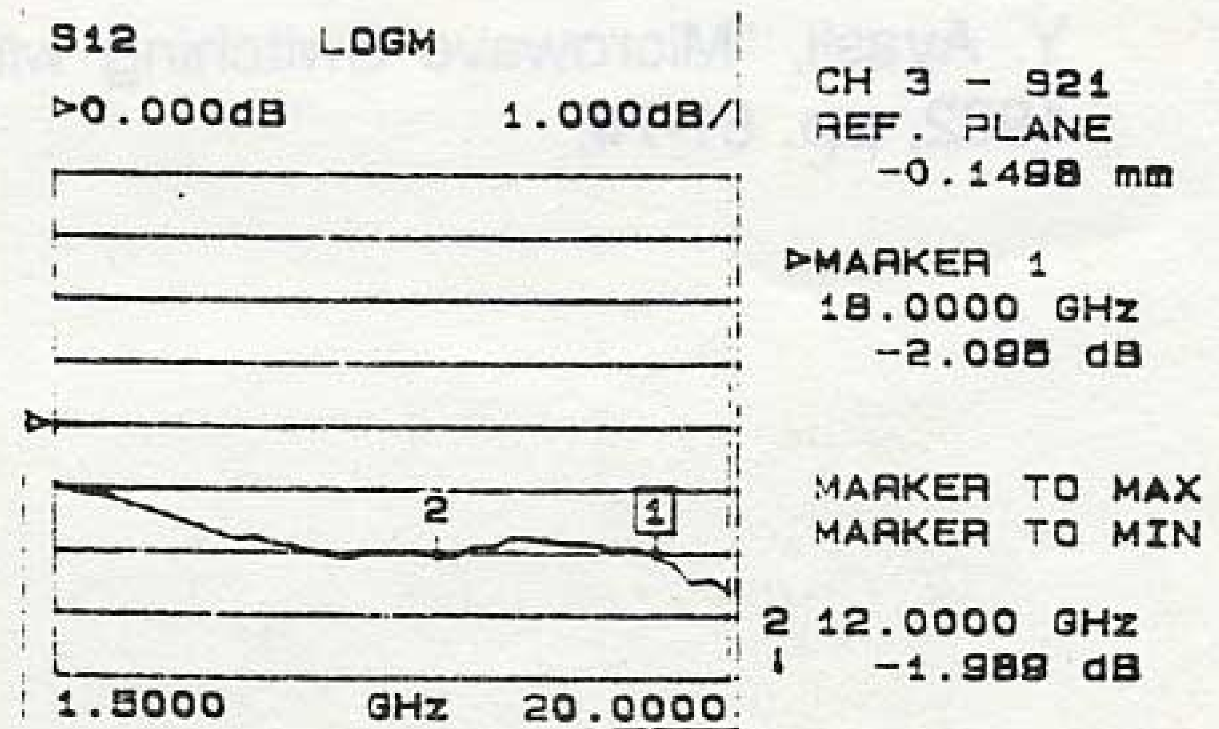


INSERTION LOSS

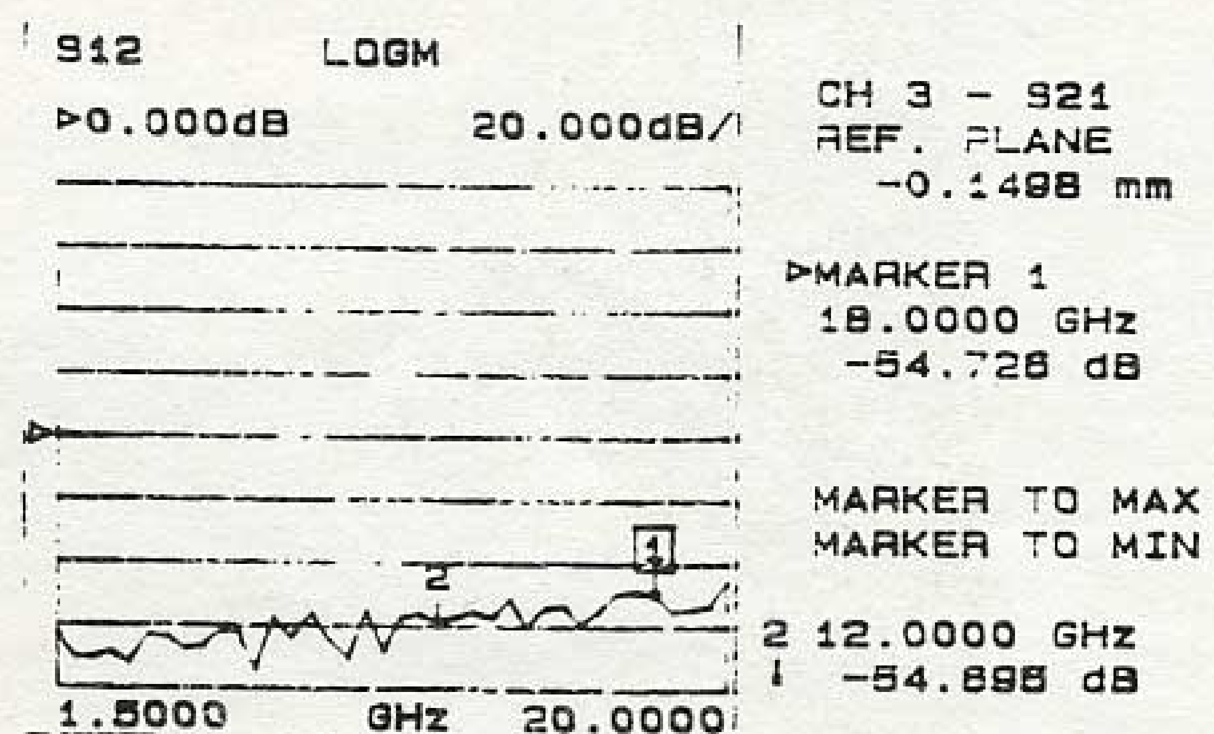


ISOLATION

FIGURE 5. SPDT PIN SWITCH RESULTS



INSERTION LOSS



ISOLATION

FIGURE 4. SPDT FET SWITCH RESULTS

CONCLUSIONS

MMIC Switches now rivals hybrid switches in performance with notorious advantages of size, speed, reliability and cost - the FET type functions well from DC through Ka-Band with slightly higher insertion loss than its PIN counterpart but with the advantage of a simpler lower power driver.

References:

[1.] Geoff Dawe, Dylan Bartle and Frank Spooner, "DC to 20GHz Monolithic GaAs FET Switches Based on Quarter-micron Gates", Microwave Journal, August 1988, pp. 116-123.

[2.] Y. Ayasli, "Microwave Switching with GaAs FETs", Microwave Journal, November 1982, pp. 61-74.