GAAS MICROWAVE OFFSET GATE SELF-ALIGNED MESFETs AND THEIR APPLICATIONS

V.G. Lapin, A.M. Temnov,
V.A. Krasnik, K.I. Petrov

State Research and Production Corporation "Istok",
Vokzalnay str. 2a, Friazino, Moskow region, 141120 Russia,
e-mail: istkor@elnet.msk.ru.

ABSTRACT

The present paper is devoted to microwave transistors, developed in SRPC "Istok". Design, fabrication and characteristics of power and low noise GaAs MESFET's and their applications are presented in this paper. The low noise MESFETs exhibit a noise figure of 1.2 dB at 15 GHz and power MESFET's show an output power density of 0.5 W/mm, with a typical power-added efficiency of 35% and thermal resistance of 10-12°C/W for a MESFET with a total gate width of 4mm.

INTRODUCTION

It's well known that microwave characteristics of GaAs MESFET's depend on the gate length. The shorter the gate the higher the operating frequency. At present microwave transistors available at the market have the gate length of 0.25÷0.5 μm and there is a tendency of its reduction down to 0.1 μm.
It's also well known, that an output power of transistors depends on the total gate width. Power transistor chips have many gate stripes connected in parallel. Multigate structure, to be effective, should have identical elementary cells working in parallel.
This requirement can be provided by identical geometry of the elementary cells and by proper device design.
The most important part of transistor technology is the process of gate defining. For this purpose, an electron beam lithography machine with the resolution of 0.1 μm or stepper is used. The electron beam machine we have at our disposal is ZBA-21 which have resolution of 0.2 μm and positioning accuracy 0.15 μm. The resolution of 0.2 μm can be obtained only in a thin (0.3 μm) layer of resist, but in defining gates "thick" (0.8-1.0 μm) layer of the resist should be used to lift off the gate metal successfully. In order to obtain a short gate length using our ZBA-21 machine, we developed our own design and fabrication technique of MESFET's.
The key features of it are:

1. Original multigate design, which allows to define gates in the channel recess by a self-aligned method and provide the offset of the gate to the source area.
2. Oblique evaporation of the gate metal to define gates set off to the source area.
3. Via holes to the source contact pads made through the "thin" (30-50 μm) GaAs, and thick backside gold metallization.
4. Separation of wafers into chips is done by chemical etching.

DEVICE DESIGN AND FABRICATION

The developed design of a power MESFET differs from usual one. The difference can be seen from Fig.1a, where the new design is shown so that you could see the difference with the usual one (Fig.1b).
Such design (Fig.1a) allows to place the gate in the channel recess by oblique evaporation, so that the gate is offset in the recess to the source area, reducing parasitic source resistance and increasing drain-to-gate breakdown voltage. All this leads to increasing gain and output power of MESFET's.
Fig.2. is a schematic illustration of our MESFET fabrication technology.
Here are the technological operations:

1. The source and drain areas are selectively metallized with AuGe/Ni/Au ohmic contacts.
2. Resist pattern is used to define mesas. Mesas are formed using shallow wet etching followed by B^+-ion bombardment.

3. The gate openings in the resist are formed by electron-beam lithography, then recesses are formed by wet etching.
4. Gate metallization oblique evaporation places the gate stripes into the channel recess, the stripes being offset to the source area.
5. The passivation dielectric is deposited and patterned by optical lithography.
6. Contact pads and "air bridges" are formed by selective gold plating.
7. GaAs wafers are lapped and polished to 100 μm thickness and then etched to 30÷50 μm.
8. Via-holes are made through GaAs substrate to the source contact pads by chemical etching using a photoresist as a mask. An etchant of our own composition is used for the purpose.
9. The back side of a GaAs wafer is metallized and selectively gold plated. The thickness of the back side metal is 15-20 μm.
10. Chip separation is done by chemical etching.

DC AND MICROWAVE PERFORMANCE

Typical DC current-voltage characteristics of a 0.5x1200 μm MESFET are shown in Fig.3. The device exhibits a very low knee voltage of 1 V and a maximum extrinsic transconductance of 170 mS/mm.
The gate-to-drain breakdown voltage is measured to be 16 V and gate-to-source to be 8 V which is sufficient for power application.
The microwave characteristics of 0.5x1200 μm MESFET are presented in Table 1 and the same characteristics are shown in Fig4.
The microwave characteristics of some transistors developed using this technology presented in Table 2.
S-parameters and the equivalent circuit of the 2250 μm transistor are shown in Fig.5.
This transistors were used in the development and production of microwave power amplifiers for communications systems.
Parameters of the amplifiers are presented in Table 3.
Power amplifiers for higher frequency band are under development now.
We have also developed low noise transistors with noise figure ≤1.2 dB and associated gain of 9 dB at 15 GHz, which were used to develop amplifiers of original coplanar design, all elements and ground metallization of which are placed on the one side of the dielectric substrate and only the MESFET and the diode chips are mounted on the dielectric substrate.
This design allows to increase the element density and to exclude hybrid capacitors and wire connections and use lumped coplanar elements.
The coplanar design allows to use the fabrication process with high throughput and reproducibility.

CONCLUSION

The microwave transistors design and fabrication technology presented in this report allowed to develop and produce a families of low noise and power microwave transistors using usual GaAs epitaxial wafers.
The transistors are widely used in several microwave devices of SRPC "Istok" and show high performance:
- Mean time to failure (MTTF) – 10^7 hours
- Thermal resistance - 10÷12 °C/W (4 mm MESFET)
- Output power density – 0.5 W/mm
- Power added efficiency - 30÷40%

Table 1. Pin-Pout characteristic of a 0.5x1200 μm device.
Idsso=400mA f=15GHz.

Pin, mW	Pout, mW	G, dB	I_D, mA	V_D	η_{add}, %
15.2	100	8.2	193	7.0	6.3
53.2	350	8.2	200	7.0	21
72.0	450	8.0	205	7.0	26
82.5	500	7.8	206	7.0	29
115.5	600	7.2	210	7.0	33

Table 2. Microwave parameters of developed transistors.

Total gate width, μm	P_{1dB}, mW	G_{1dB}, dB	$I_{DS}xV_{DS}$, mAxV	f, GHz	η, %
1200 (18x66)	600	7.0	200x7	15	30
2250 (18x120)	900	7.0	300x7	12	35
4000 (32x125)	2100	8.0	600x8	8	37

Table 3. Microwave parameters of power amplifiers.

Type	f, GHz	• p, dB min	Δ• p, dB max	Pout, W	U x I, V x A
M1015	1..1,5	30	2	12	+8,6x6; -5x0,2
M1420	1,4..2	30	2	12	+8,6x6; -5x0,2
M3439	3,4..3,9	33	1	3	+8x1,8; -5x0,2
M1020-4	1..2	20	4	6	+9,5x3; -5x0,2
M3439-10	3,4..3,9	13	1	10	+8x4; -5x0,2
YM51115	3,4..3,9	40	1	15	+8x10; -5x0,4
YM1113	5,67..6,17	36	1	10	+8x7; -5x0,3
M8184	8,1..8,4	40	1	11	+7,5x6; -5x0,2

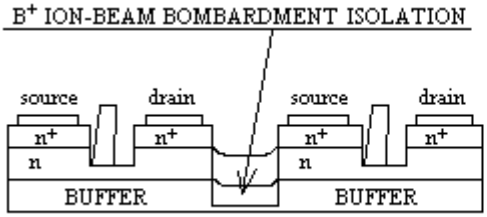


Fig.1a. New design of multigate MESFET's.

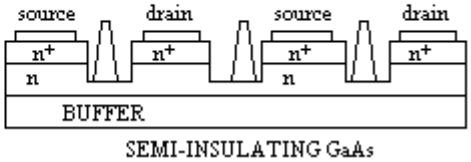


Fig.1b. Usual design of multigate MESFET's.

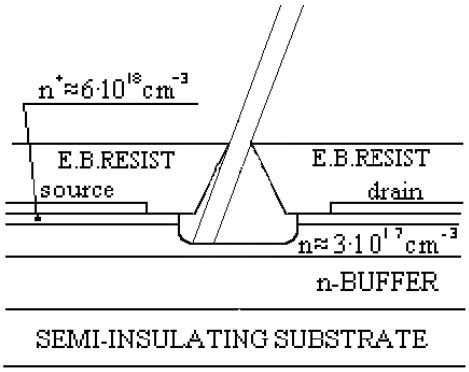


Fig.2. Schematic illustration of MESFET fabrication technique by oblique evaporation.

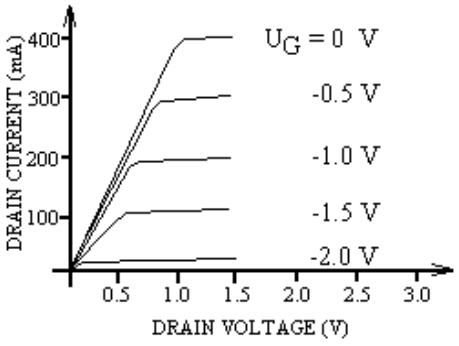


Fig.3. Typical DC current-voltage characteristics of a 0.5x1200 μm device.

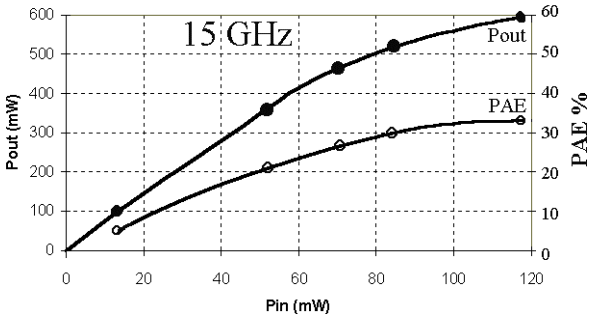
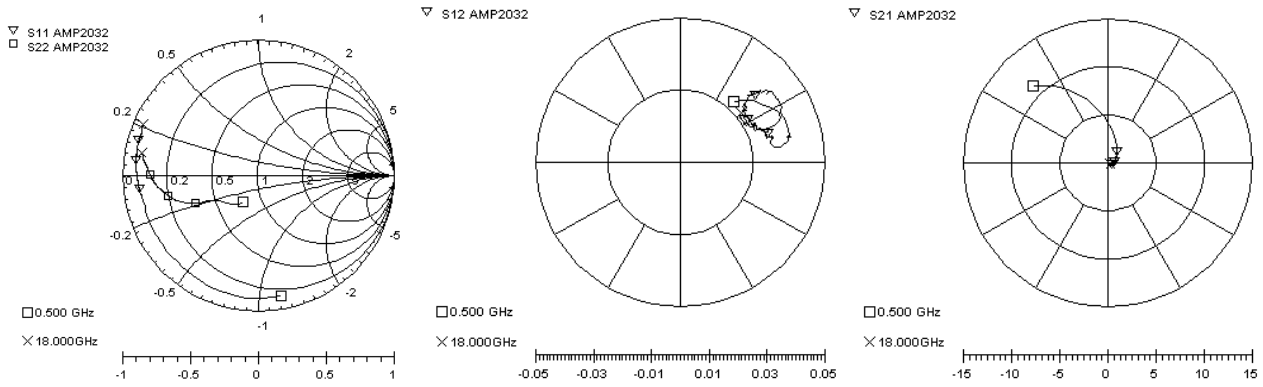
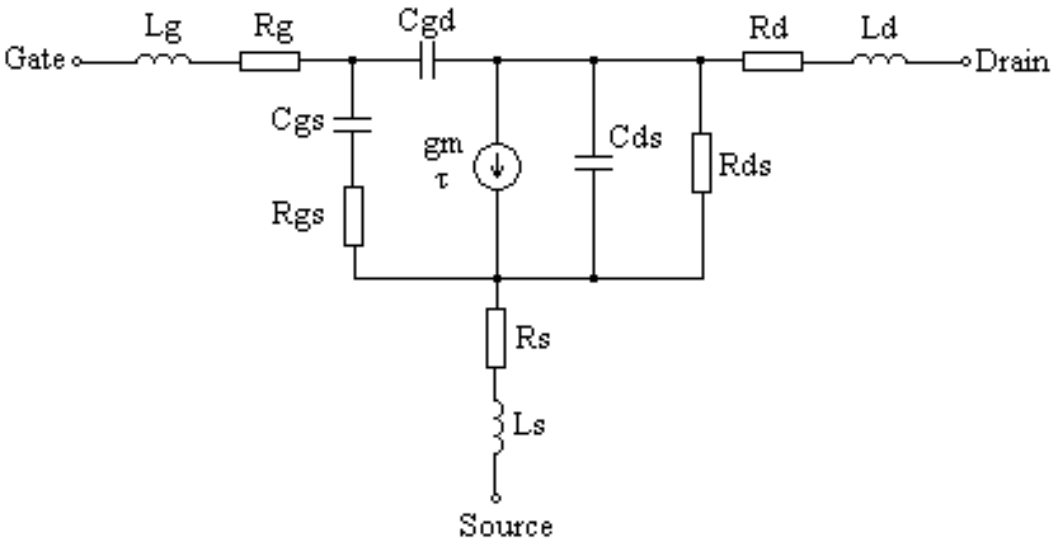


Fig.4. Pout and PAE versus Pin for a 0.5x1200 μm MESFET.





gm	365.14	mA
τ	4.56	ps
Rg	1.467	Ω
Rs	0.416	Ω
Rd	2.42E-4	Ω
Rgs	0.13	Ω
Rds	43.77	Ω
Cgs	4.153	pF
Cgd	0.16	pF
Cds	0.765	pF
Lg	0.106	nH
Ls	0.0115	nH
Ld	0.119	nH

Bonding wire condition

	Number (pcp)	Length (Approx) (mm)	Dia (mm)
Drain	3	0.4	18
Gate	3	0.4	18

Fig.5. S-parameters and the equivalent circuit of the 2250 μm transistor.