Push-Push X Band GaInP/GaAs VCO with a Fully Monolithic Microstrip Resonator

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Abstract — **In this paper the design of a VCO using GaInP/GaAs HBT technology is presented. The VCO is designed to be part of a PDH point to point radio system. To achieve low phase noise performances GaInP/GaAs HBT technology and push-push topology have been chosen. The MMIC includes predistorters to emphasize the second harmonic, $f_0/2$ prescalers for PLL locking and buffer amplifiers. A fully monolithic microstrip resonator is coupled with integrated varactors to achieve the specified tuning bandwidth. Phase noise, bandwidth and power measurements will be also presented.**

Index Terms — **Heterojunction bipolar transistors, Microstrip resonators, Push-Push, Phase Noise, Voltage Controlled Oscillator.**

I. Introduction

As the market of the PDH and SDH radio links has been spreading out during the last ten years, the need for stable frequency references is a problem of first concern for the microwave radio link industry. In fact, the exponential grow of the portable communications market has driven to the birth of many wireless telephone companies that built up their own networks all over the Europe to provide their costumers a stable service. Commercial handsets can now handle not only voice data, but even images and video: therefore the radio link has to deal with much more complex digitally modulated signals and as a consequence the transmitter needs a larger bandwidth and a more precise frequency reference. The goal for VCO designers is to achieve the specified bandwidth within the respect of demanding phase noise performances. The lower is the synthesizer phase noise the bigger is the bandwidth efficiency of the system.

In this paper we describe the design and testing of a VCO for a PDH 52GHz radio link. The oscillator operating frequency is between 8 GHz and 9 GHz with a tuning bandwidth of 400MHz. The VCO exhibits bandwidth and phase noise performances that make it suitable for any kind of medium capacity digital radio link with modulation schemes up to 16QAM. These good performances are achieved with a fully monolithic design thanks to the oscillator push-push topology [1], a microstrip integrated resonator and the low noise characteristics of GaInP/GaAs HBT technology.

The paper is organized as follows: in section II a short description of the systems and its specifications are given; section III describes the MMIC design approach; section IV is dedicated to the design environment, while in section V we will give information on the circuit implementation.

Measurements data are displayed in section VI, while in section VII includes some final conclusions and illustrates the future activity on this application.

II. System Description and Specification

The MMIC is part of a 52 GHz radio link system. The circuit implements not only a simple VCO, but a prescaler block and a gain stage as well. The design goal is to implement a VCO with central band output frequency f_0=8.5GHZ, output power between 5 and 10dBm, 350MHz tuning bandwidth and phase noise around –80dBc/Hz across all the tuning bandwidth. As the VCO is part of a PLL, an $f_0/2$ output (with at least –5dBm output power) was requested to adopt an integrated prescaler for the first down conversion. Therefore the MMIC is not only a simple VCO but really a multifunctional chip.

III. MMIC Design

An overall description of the chip blocks topology and functionality is useful to understand the design process:

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A. Chip description

Looking at the block diagram in figure 1, we can distinguish the two symmetrical oscillators (dashed lines) that are coupled to implement the Push-Push topology [1][2]. The two circuits oscillate at half the output frequency and are followed by two prescaler buffers that make the $f_0/2$ output available to and external PLL loop.

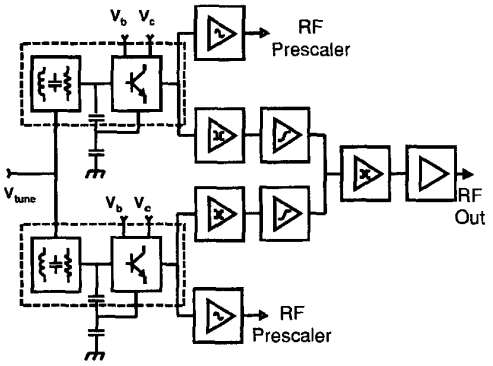

Fig. 1. Functional block scheme of the VCO MMIC.

Before coupling in anti-phase the twin oscillator outputs, the reference signals pass trough a separator and a predistorter that emphasizes the second harmonic (at f_0). In fact we chose the large signal operating point of the oscillator core transistors to be as "linear" as possible: this choice of a small compression working point guarantees good phase noise performances, but, as a consequence, we need a predistorter to increase the second harmonic that is the useful signal.

B. Oscillator core

The oscillator core is the key part of the MMIC.

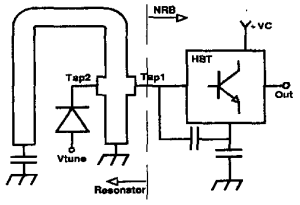

Fig. 2. Oscillator core schematic: negative resistance bipole and resonator.

The oscillator topology is a classical negative resistance one, so we can distinguish the negative resistance bipole NRB from the resonator part (figure 2). The two oscillator cores are connected at one resonator end in the classical Push-Push topology (figure 3) which suppresses even mode oscillations. The NRB is a single transistor in a Colpitts configuration, while the resonator is implemented by means of a $\lambda/4$ microstrip resonator coupled with a row of varactor diodes to achieve the required tuning bandwidth. The microstrip resonator guarantees a better Q factor rather than the classical LC tank with lumped elements. For space requirements the resonator was folded and terminated with a 0.2pF lumped grounding capacitor in order to decrease its length. The other end of the resonator is terminated to ground trough a via hole.

The NRB was designed trough linear and non linear simulations to guarantee the desired small-signal gain for the oscillation start-up, and a suitable large signal operating condition. In fact, if on one side a deep gain compression gives amplitude stability, it also degrades the phase noise: therefore a good trade-off choice was adopted.

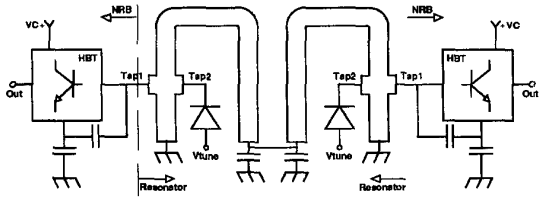

Fig. 3. Push-Push topology for the two oscillator cores.

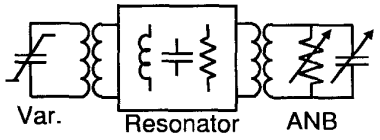

Fig. 4. Equivalent circuit of the negative resistance oscillator.

The same considerations were applied when choosing the oscillator small signal loop gain. Once the NRB part is designed, the loop gain can be manipulated varying the transformation ratio between the active part and the resonator. As we can see from figure 2, the resonator has got a double tap on opposite sides of the microstrip line. The position of tap2 tunes the coupling with the varactor diodes, while the position of tap1 regulates the coupling coefficient with the NRB. So, by modelling the microstrip resonator with an RLC network, the oscillator core can be described with the equivalent circuit in figure 4. Moving the tap along the microstrip, the transformation ratio with the NRB changes, therefore, accordingly, the resonator equivalent resistance and the loop gain change. So the

choice of the tap position regulates two important design parameters:

a) the small signal gain for oscillator start up
b) the equivalent resistance shown to the NRB under large signal conditions, therefore settling the transistor working point

We chose tap 1 position in order to have a small signal odd order loop gain of 1.8 that seemed to be a good compromise between a good margin for the start up and good phase noise performances. The other tap (tap2) regulates the coupling with the varactor diodes. To maximize the diodes tuning effect they should be connected at the end of the resonator near the 0.2pF capacitor: in this way all the equivalent capacitance of the varactor is shunted to the RLC resonator equivalent.

Unfortunately this situation corresponds to the maximum swing of the signal voltage amplitude on the varactors, driving them into breakdown or forward conduction. The tap introduces a transformation ratio between the resonator and the varactors and resolves these problems: the drawback is a decrease of the diodes tuning capacity.

C. Predistorters and buffers

Predistorters are implemented by biasing two HBT amplifiers almost in class B operating point. In this way the transistor operating point is highly nonlinear and the output signal provides a high second harmonic contribution.

The transistor is in common emitter configuration with an emitter degeneration resistor to guarantee bias stability. The base bias is implemented by means of an integrated resistive network. Predistorters are separated from the oscillator core output by means of separator buffers. These buffers have the same common emitter configuration and assure that the oscillating device won't be affected by load pulling due to the predistorters highly nonlinear input impedance.

D. Prescalers

As previously stated, the prescalers provide at the output the $f_0/2$ reference, extracting it directly from the single oscillator output before the push-push coupling.

Prescalers have got the same common emitter topology of the separator buffers and provide 0dBm output power signals.

E. Microstrip combiner and Amplifier stage

The signals provided by the two twin oscillators and manipulated by the predistorters are added out of phase by a simple microstrip combiner. In such a way, the first harmonics ($f_0/2$) are almost totally suppressed, while the second ones add in phase and produce the output signal at f_0. As the system requires at least a 5dBm output power, a final amplifier stage was designed. The amplifier has a common emitter configuration with emitter degeneration resistor for bias stability. Differently from the buffers and predistorter stages, as the gain is of first concern, the emitter resistor is partitioned and partially by-passed by a shunt capacitor to avoid gain degradation. The amplifier is biased in class A. The input and output networks are synthesized respectively for maximum gain and maximum output power.

IV Simulation Environment

The MMIC design was carried out in Agilent ADS2002 Environment using UMS foundry design kit and manual. The microstrip resonator was simulated by means of Momentum electromagnetic simulator.

Simulations at different temperatures and accounting for parameter spreading were performed to check the design robustness, thanks to the thermal model and process spreading information available in the foundry design kit.

Phase noise simulations were performed using the low frequency bias dependent noise model provided by the foundry for the active devices.

V. Circuit Implementation

The circuit was manufactured using an industrial GaInP/GaAs HBT process by UMS. This process is a 2μm finger width and is optimized for power amplifiers and low noise oscillators applications from C up to Ku frequency bands. The process also includes via holes through the 100μm thick substrate, MIM capacitors, resistors, spiral inductors and air-bridges.

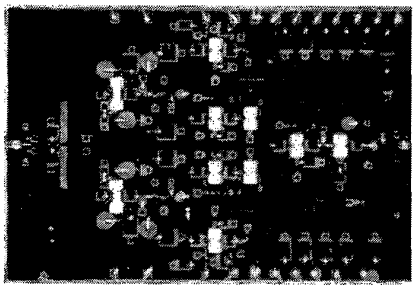

Fig. 5. Photograph of the complete MMIC 5 x 3.38 x 0.1mm

The oscillator core devices are 6 finger transistors with 30μm finger length, while all the other transistors used for the amplifier, buffers and prescalers are 2x30μm devices. We chose a bigger periphery transistor as the oscillating device because we had indications from the foundry and from previous literature that a reasonably big periphery gives better low frequency (1/f) noise performances. The chip dimensions (5x3.38x0.1 mm^2) are quite large, but nothing was done to minimize the chip size the main objective being the success at the first run: many dimensions can be quite easily shrunk in an upgraded design version.

VI. VCO Measurements

The MMIC was mounted on a test jig to measure its performances. The chip is biased by microstrip lines on an alumina substrate that carry the dc current from an FR4 board to the MMIC bias pads around the chip perimeter. Bonding wires and ribbons connect the GaAs chip pads to the microstrips on alumina and from the latter to the FR4 dc board, respectively. The FR4 board with SMT lumped components implements the bias voltages and inductor-capacitor low pass filters to cut the low frequency noise at a few hundred hertz. A noise-free bias is particularly important for the oscillator core transistors and the varactors.

SMA cables connect the prescaler output to an external PLL in SMT technology. In figure 6, bandwidth and power measurements are displayed. The VCO exhibits 400MHz pretty linear tuning bandwidth with an output power that fulfills specifications.

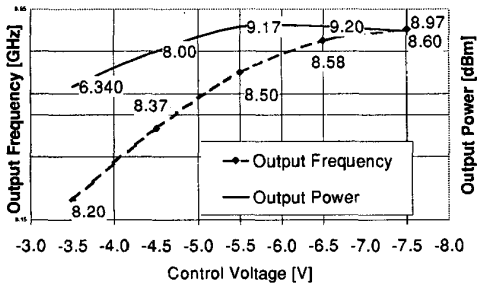

Fig. 6. VCO Bandwidth and power measurements.

In figure 7 the SSB phase noise at 10KHz from the carrier across all the bandwidth is presented. The VCO exhibits a phase noise better than the addressed value of -80dBc at 10KHz except for a couple of bias points. Those tuning points correspond to the most selective part of the C/V varactor characteristic, where the oscillator frequency sensitivity to the low frequency voltage noise is very high.

We noticed a difference between phase noise simulations ad measurements of 5dB at least. This discrepancy can probably be overcome with an upgraded version of the noise model that is under study.

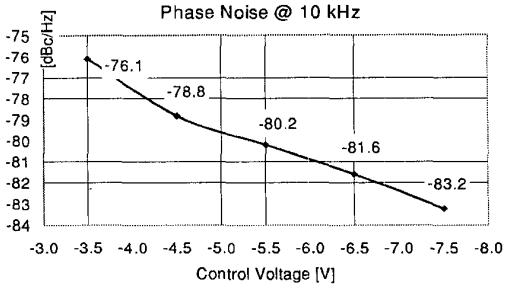

Fig. 7. VCO phase noise measured performances.

VII. Conclusions an Future Work

The design and testing of a fully monolithic VCO at X band in Push-Push topology has been presented. To maximize the quality factor, a microstrip resonator rather than a classic LC tank has been chosen. The resonator is tuned by means of integrated varactors. The MMIC includes prescalers at $f_0/2$, predistorters and buffer amplifiers. The VCO is assembled in a module with external DC bias networks and is locked into a PLL system. Measurements exhibit reasonably good agreement with circuit simulations and almost fulfill the system specifications at the first foundry run. The phase noise discrepancy between simulations and measurements could be overcome by using a new low frequency noise model under development. A second foundry run with an improved microstrip resonator is under delivery.

Acknowledgement

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