TOWARDS FULLY INTEGRATED CMOS RF RECEIVERS

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ABSTRACT

The evolution of the mobile telephony is demanding new multi-function terminals (cellular and cordless phones, GPS, pagers) compatible with a variety of standard (GSM, DCS, DECT, CDMA). At the same time the reduction of cost, size and power dissipation is mandatory. All this requires an higher integration level for the RF part, that is presently using a big number of components. This explains the big research effort put in silicon RF circuits particularly in CMOS technology. In this paper the state of the art of CMOS RF circuits is outlined. In particular some results regarding critical building blocks obtained by the STMicroelectronics and Pavia University research team are given. Future developments and the progress needed to successfully implement them are also pointed out.

INTRODUCTION

The evolution of wireless communication is progressing at a faster and faster pace. In particular, the wireless cellular terminal is becoming much more sophisticated with the advent of third generation systems (UMTS). Specifically a third generation terminal will have to be multifunction (e.g. voice, fax, mail, internet, GPS, etc.) and multistandard (e.g. GSM, DCS 1800, WCDMA, etc.). At the same time the key requirement for the terminals is to preserve (or even improve) cost, form factor and power dissipation. This forces to reduce the number of components, passive and active, making up the system.

The two conflicting requirements of increased complexity and simpler implementation can only be reconciled by increasing the level of integration, especially of the RF front-end that should become highly programmable (digitally if possible). The prime candidate technology for these highly complex system-on-a-chip is silicon BiCMOS. This because it combines the availability of bipolar devices (may be SiGe) for the front-end and CMOS for the back-end. However, the rapid evolution of deeply scaled digital CMOS technologies has created devices with characteristics (f_T, f_{MAX}, etc) that challenge that of the bipolar ones. Due to this and given the potential economic advantage of using standard CMOS a great amount of research in RF CMOS circuits has spurred at both university and industry level.

In addition to cellular phones other types of wireless terminals are being introduced. In particular, wireless LAN (e.g. Blue-tooth, Home–RF etc.) have the potential for a very rapid growth. In these cases the motivation for "single chip solutions" is even stronger (for cost reasons) and more likely to occur in the near term given their less stringent standards.

Over the last few years, we have seen examples of the tendency outlined above typically in terms of RF front-ends in either BiCMOS or CMOS and in some cases even complete transceivers on a single chip. This has occurred first at conferences or in the technical literature but more recently also as commercial products.

One of the first examples is an RF front-end for a GPS system, which being a one way system, only requires the receive portion. Still in this case the problem of sharing the same substrate between analogue and digital portions is not addressed. More recently a complete transceiver for digital cordless systems has been integrated on a single CMOS chip by Level One Communications (Fig. 1, [1]). This demonstrates the possibility of true system-on-a-chip although the system requires a very small power in the transmit section and has fairly relaxed specs. On the other hand, the most aggressive attempt at full integration of an RF transceiver front-end (excluding however the digital portion) is that proposed at UC-Berkeley presently under testing. This chip is the first that attempt to put together both a GSM/DECT receiver with the full transmitter including a high power (few Watts) power amplifier (PA).

In the following some of the key building blocks making up an RF receiver are discussed in the context of a pure CMOS implementation. All the examples are taken within the designs performed at the joint research centre between STMicroelectronics and University of Pavia.

CMOS BUILDING BLOCKS

On-Chip Inductors.

The design of high quality integrated inductors is a key point for the realisation of Radio Frequency selective amplifiers/filters and voltage controlled oscillators (VCOs).

Inductors in the range of 1nH to 10nH can be integrated and they are commonly realised as spirals using the top metal layer (Figure 2, [2]). In this implementation the causes of losses are of three kinds:

- finite conductivity of the metal itself (electric losses, see Q_{MET-EL} in Fig. 3)
- electric coupling with the substrate (electric substrate losses, see Q_{SUB-EL} in Fig. 3)
- magnetic coupling with the substrate (magnetic substrate losses, see $Q_{SUB-MAG}$ in Fig. 3)

The quality factor (Q) degradation due to each contribution is reported in Fig. 3 for a typical CMOS on-chip inductor. Electric losses con be reduced using multi-metal-layer or collapsing the two top layers into a single thicker metal. In this way a thickness of about 2μm aluminium is obtained with a resistance of 25mΩ. . The skin effect is in fact not appreciable at a frequency of a few GHz. In the near future the availability of thick copper conductors (used to increase the speed of the digital portion) will make these losses lower.

Substrate losses (both electric and magnetic) are due to the finite resistivity of the silicon substrate which is not very high (as compared to GaAs). The resistivity depends on which kind of silicon wafers are used, but lowly doped wafers with a value around 10Ω·cm are becoming a sort of standard for RF CMOS applications.

A solution for reducing electric substrate losses is the interposition of a patterned shield between the metal and the substrate which acts as an high Q capacitor for the electric field but does not interfere with the magnetic field. The shield is realised with conductive layers such as N+ or siliced polysilicon.

An efficient solution to reduce magnetic losses in standard CMOS processes has not been found yet. Some prototypes have been realised using special etching and oxidation techniques to put a thick silicon-dioxide layer (40μm) under the inductor. In this way the quality factor grows up to 20 @ 2GHz.

Voltage controlled Oscillators.
The oscillator phase noise required for RF applications force to use LC-type VCOs instead of the more classical and compact solutions such as ring or relaxation oscillators.

In LC-type VCOs the performance depends strongly on the quality of the passive inductors and varactors used. The most popular solution for integrated oscillators is the cross coupled differential pair which realises a differential negative resistance to compensate the losses in the LC tank.

The example reported here (Fig. 4, [3]) is slightly different since the negative resistance is implemented using two cross coupled pairs (N and P) shunted together. In principle this architecture improves the phase noise by 3dB or, equivalently, gives the same phase noise with half the current. This topology is only suitable for CMOS implementation since very high speed PNP are seldom available. The design is determined by the quality factor of the tank, the voltage supply and the current consumption. In fact for a given current I, the value of the inductor is chosen in such a way that the output voltage swing is maximum for the given topology and supply voltage. This can be easily done since the equivalent tank resistance is given by $R_{Tank}= \omega_0 \cdot L \cdot Q_{Tank}$ and, at the first order, the voltage swing is equal to $I \cdot R_{Tank}$.

From the value of the inductor, the value of the capacitor is determined by the oscillation frequency: $\omega_0 = 1/\sqrt{L \cdot C}$. The C value should not be too small compared to parasitics at the output nodes because this limits the tuning range and the VCO gain. The transconductance of the differential pairs is chosen 2 or 3 times higher than $1/R_{Tank}$ to allow start-up. With these design choices, the value of the MOS overdrive is well defined and depends only on the chosen topology and the supply voltage.

The reported oscillator has been implemented in two version: using bondwire or BGA inductors. In both case the Q_{Tank} can be assumed around 15 and it is limited by the integrated varactor. The current consumption is 1mA from a 2V power supply. The phase noise performance can be measured using the following figure of merit:

$$FoM = 10 \cdot \log[(f_0/\Delta f)^2 \cdot (1/(P \cdot £(\Delta f))] \quad (1)$$

which normalises the phase noise (£(Δf)) to the oscillation frequency (f_0) and to the power consumption P, in mW.

As can be noted in Fig. 5 performance of this and in general CMOS oscillators are comparable or better than bipolar and competitive with discrete solutions.

Low Noise Amplifiers.
In a Radio Frequency receiver the first amplification stage (LNA) accomplishes two functions: the input termination and the low noise amplification of the signal coming from the antenna.

The topology of Fig. 6a [4] is often used to implement these functions. This circuit has the property to show a real impedance at the input terminal and, at the same time, to realise a source impedance for the active device close to its optimum noise impedance. Both goals are achieved in a narrow frequency band centred around $1/\sqrt{C \cdot (L_S+L_G)}$, but this is not a limitation for the narrow band signals typical of the communication standards. The input pair is loaded with a resonant LC tank.

Exploiting the availability of the good P-channel transistor of CMOS processes (with tech. scaling the speed of Pmos is getting closer to Nmos) a novel input stage has been studied and integrated in the front-end of a pager using the Reflex standard. The resulting circuit in its differential form is shown in Fig. 6b. The measured performance are the following: current consumption 8mA from a 2.7V power supply, NF of 2dB@900MHz, Voltage gain of 22dB and IIP3 of -3dBm.

Again this results are achievable only if the reactive elements of the input network have a good Quality Factor. For this reason in the described prototype the gate inductors are partially external. The only other on-board component is the single-ended to differential BalUn that is necessary to use a differential amplifier which is more immune to disturbances.

Example of monolithic GPS Front-End

Finally, an example of RF analogue front-end for GPS application is reported. GPS has been chosen as test vehicle since it is, at present, one of the more realistic standard to be fully integrated on an industrial scale together with the DSP. In fact, the absence of transmission and the use of an active antenna (that gives an input signal around $1\mu V_{RMS}$) make cross-talk more manageable.

The leit-motif of the project has been to integrate all components on chip. The total amount of gain required for LNA and Mixer was 40dB and this has been rarely realised without IF amplification. The chosen architecture for the LNA has been the one described in the LNA section and shown in Fig. 6a while the implemented Mixer structure is very similar to a classical Gilbert-Cell with the exception of the Pmos-Nmos input stage that allows to achieve higher gain for a given power consumption (Fig. 7). The prototype has been integrated in a 0.35µm CMOS technology with passive inductors having a quality factor of 8 @ 2GHz. The shields described in the previous section have been used. The overall measured performance of the circuit are shown in the following table. The reported power consumption includes the IF buffers at 150MHz [6].

f_{in} [GHz]	f_{out} [MHz]	Gain [dB]	S_{11} [dB]	NF [dB]	IIP3 [dBm]	Z_{out} [Ω]	Power [mW]	V_{DD} [V]
1.575	150	39.7	-12.5	3.8(DSB)	-25.5	70	30	2.8

Table. 1 GPS Front-End Overall Performance.

CONCLUSIONS

The paper has given an overview of the critical building blocks of a wireless receiver showing the achievable performance using standard CMOS technology. The natural evolution is combining all of these blocks on single substrate ultimately together with a digital back-end. However to be able to achieve this goal some key concepts and methodologies must be further developed. These lay at the system level (e.g. self-calibration, adaptation etc.), at the architectural level (e.g. direct conversion, wide-band conversion etc.), at the circuit level (e.g. current reuse techniques etc.), at the technology level (e.g. active and passive devices improving), at the simulation and modelling level (e.g. cross-talk models).

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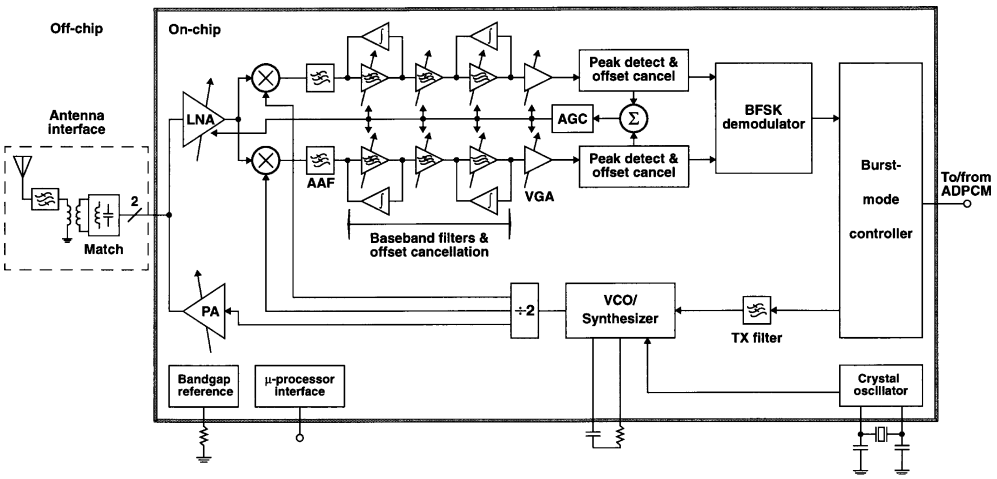


Figure 1. Example of an integrated commercial product (LevelOne).

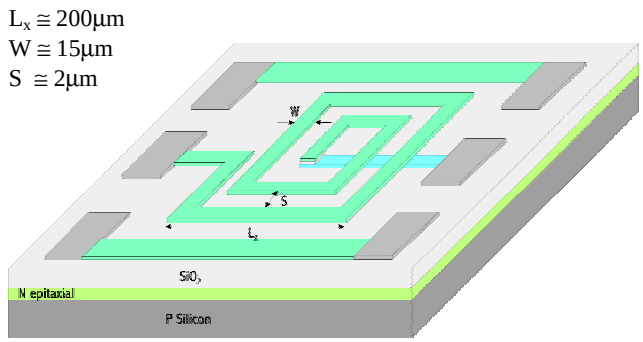


Figure 2.Typical On-Chip Inductor

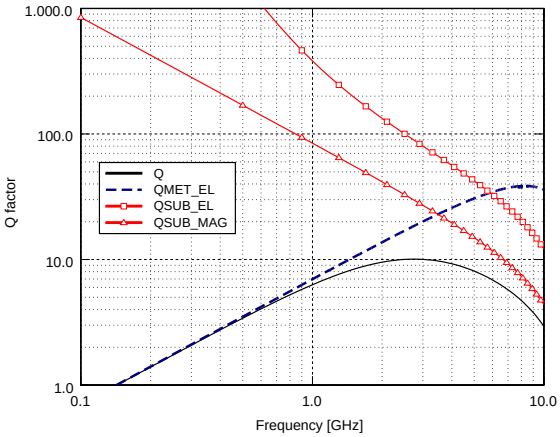


Figure 3. Q degrading contributors in CMOS inductors

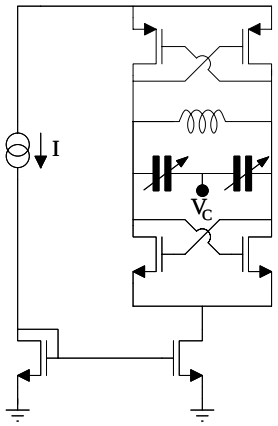


Figure 4. VCO Schematic

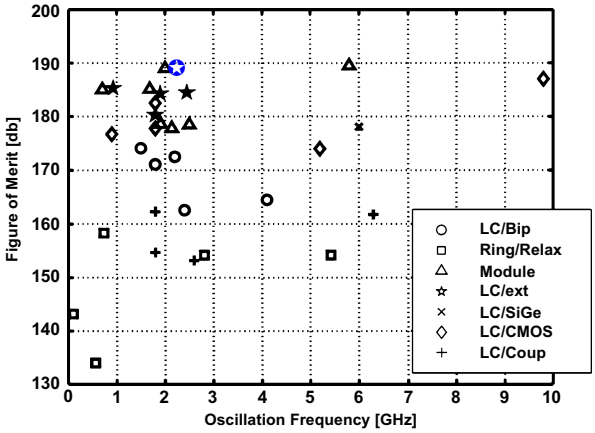
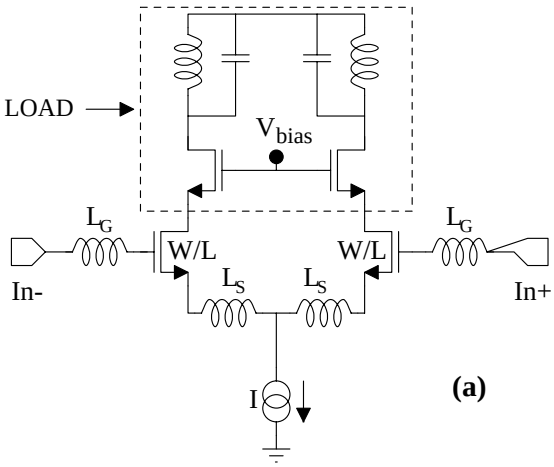


Figure 5. FoM of different oscillators (✪presented prototype)



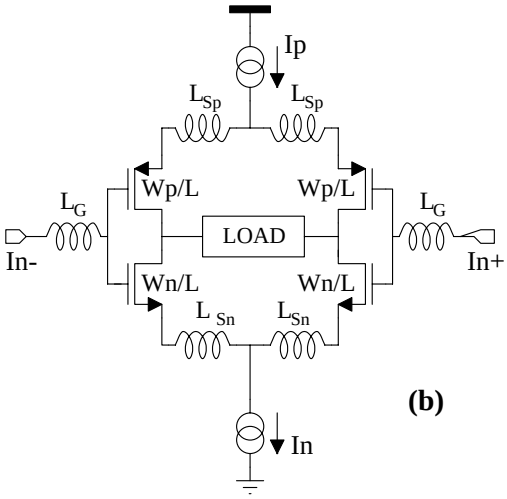


Figure 6. a: Classical topology, b: Novel solution.

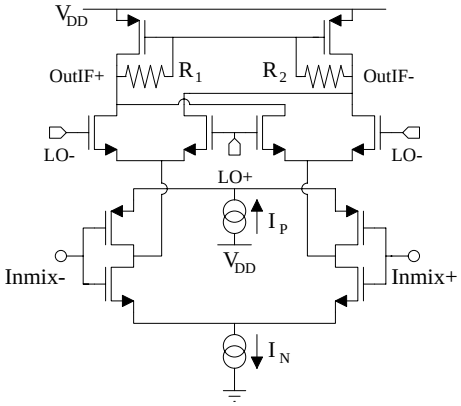


Figure 7. Mixer stage of the presented GPS front-end