

A L-BAND 50-WATT GaAs POWER FET WITH 58% POWER ADDED EFFICIENCY

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Abstract

High efficiency 50W GaAs power device has been developed using two high breakdown voltage GaAs FET chips that have an AlGaAs/GaAs heterostructure. Circuit designing considerations include the termination of the second-harmonics for improved power added efficiency. The resultant output power at the 3dB gain compression point is 47.0dBm with 58% power added efficiency (PAE) and 15.0 dB linear gain at 1.6GHz.

To the authors' knowledge, this is the highest efficiency for a 50-watt GaAs device in the industry.

1. Introduction

Recently the demand of higher power amplifiers has expanded into various applications W-CDMA base-station for mobile communications and high-speed satellite communication systems.

For L and S-Band applications, over 100W devices have been reported for push-pull configurations [1-2], but there are no reports for single ended high efficiency devices over 30 watts for L and S band devices [3-4].

This paper demonstrates that by optimizing the unit gate width against the gain and harmonics behavior, 50 watt high efficiency GaAs FET devices were obtained.

2. GaAs FET chip consideration

The feature of GaAs FET chip is an AlGaAs/GaAs heterostructure and gold gate metal to obtain high breakdown characteristics and high reliability.

To achieve high power added efficiency (PAE) without changing FET fundamental structure, higher gain and effective harmonic termination are required. Because they are associated unit gate width, the best unit gate width was determined from the study of the FET samples with different

unit gate width from 200um to 1000um with close total gate width. Maximum available gain (Gamax) and effectiveness of second-harmonic termination was evaluated by S-parameters measurement and load-pull measurements.

The results are shown in table 1. Maximum available gain decreases by approximately 8dB along with unit gate width from 200um to 1000um. 2 dB-compressed gain of 11dB is minimum permissible value to achieve the acceptable PAE. From our experience, maximum available gain at 7GHz is roughly 6dB lower than the linear gain at L-band, so unit gate width have to be less than around 600um. Maximum drain efficiency of 80% was obtained from up to 400um unit gate width samples since the second harmonic termination is much effective. Harmonic termination effect was confirmed on the sample with unit gate of 600um but no effect was observed on the 1000um sample.

From these measurements, it was determined that 600um is the maximum width for gain and effective second harmonic termination. This resulted in the design of a 1.1mm x 3.6mm chip with a total gate width (Wtg) of 86.4mm with a total of 144 gate electrodes and twelve gate pads as shown in figure 1.

Unit Gate Width [um]	Gamax [dB] @7GHz	Drain Efficiency with Second Harmonic Termination @1.6GHz
200	12.6	80%
400	10.5	80%
600	7.5	75%
1000	4.8	70%

Table 1. Unit gate width dependency of Gamax and second harmonic termination effect.



Figure 1. Top view of GaAs FET chip. Unit gate width is 600 um and total gate width is 86.4mm. Chip size is 3.6mm x 1.1mm.

3. Circuit design

A single-ended 50watt device was designed using the two FET chips in parallel. Based on the harmonic load-pull measurement using a unit FET cell with a one twelfth gate width of one chip, it was found that the best source and load impedance for maximum PAE at 1.60GHz is $5.0+j11.6$ and $10.8+j14.0$ ohms, respectively. Best second harmonic phase angle of approximately -30 degrees was also obtained as shown in figure 2.

Using typical combining techniques, the FET unit cell data was combined to determine the impedance of one chip. This information was used for the single ended design shown in figure 3.

Substrates with a high dielectric constant of 90 were used for the output transformer. The divider and combiner fabricated on alumina substrate were designed to additionally reduce its size by the

shunt capacitor. This reduced the size of the matching structures. To reduce bias losses, 20 μ m thick gold microstrip lines were used for the output substrates. The overall device size including the input and output leads is about 14mm x 20mm.

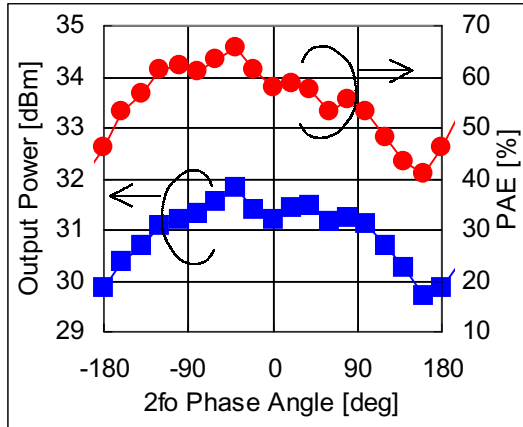


Figure 2. Harmonic Load Pull measurement results of the 600 μ m x 12 fingers unit FET cell at $V_{ds}=8V$. Fundamental frequency is 1.6GHz.

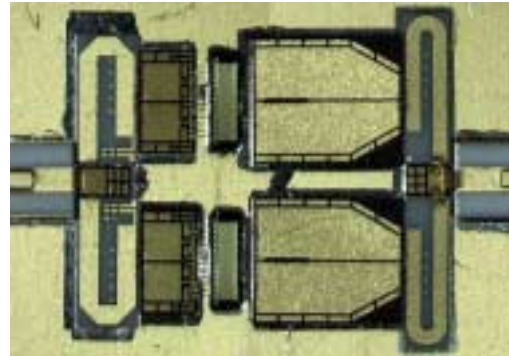


Figure 3. Photograph of 50W GaAs FET device using two FET chips. Device size is 14mm x 20mm.

4. Electrical performance

The saturated drain current (I_{dss}) and pinch-off voltage (V_p) is 26A and -2.1V, respectively. And the gate breakdown voltage (V_{gdo}) is 32V at gate current $I_{gd}=86.4mA(0.5mA/mm)$.

Figure 4 shows the output power and power added efficiency (PAE) of the 50 Watt device as a function of input power at $V_{ds}=9.0V$, 1.625GHz. Output power at 3dB gain compression point of 47.0dBm (=50W) with 58.1% PAE was obtained. Linear gain was 15.0 dBm. Figure 5 shows the P3dB and PAE as a function of frequency at $V_{ds}=8$ and 9 Volt. Higher PAE than 57% was obtained within the 50 MHz bandwidth at $V_{ds}=8V$.

5. Summary

An L-band 50watt high efficiency single-ended GaAs power FET device has been developed. This device has good linear gain of 15.0 dB and high power added efficiency of 58%.

Many communication systems should benefit from the high performance obtained from this device.

6. Acknowledgement

The authors are grateful to K. Ebihara and H. Takahashi for helpful discussion. We also thank T. Iida for taking photos, and T. Igarashi and H. Haematsu for this chip preparation.

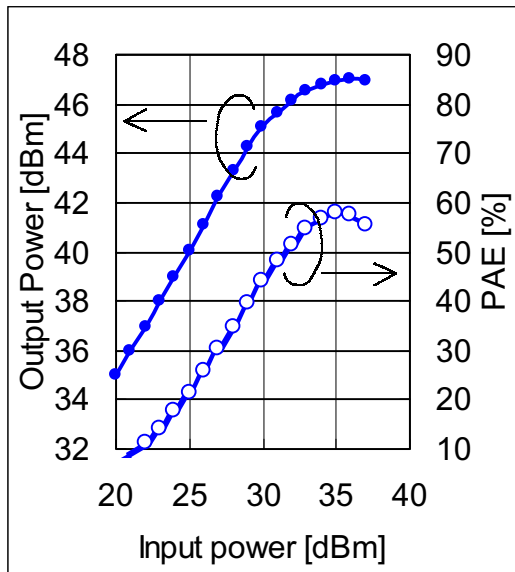


Figure 4. Output power and power added efficiency versus input power at $V_{ds}=9.0V$, $1.625GHz$.

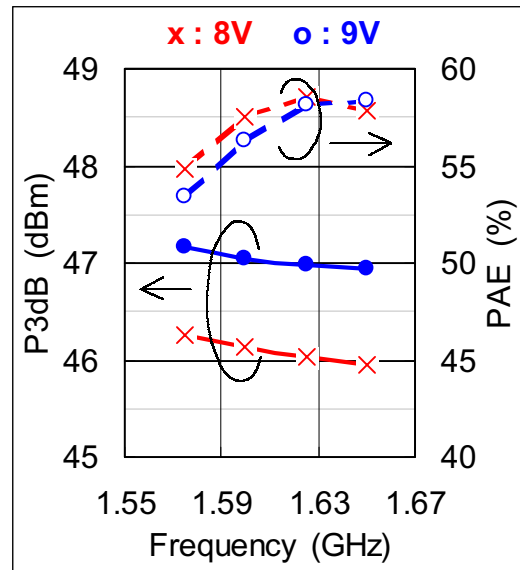


Figure 5. Output power at 3dB gain compression point and power added efficiency versus frequency at $V_{ds}=8.0$ and $9.0V$

7. References

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