BREAKDOWN AND HIGH-FIELD RELIABILITY ISSUES IN HETEROJUNCTION FETs FOR MICROWAVE POWER AMPLIFICATION

R. Menozzi

Dipartimento di Ingegneria dell'Informazione, University of Parma
Parco Area delle Scienze 181A, 43100 Parma, Italy
e-mail: r_menozzi@ee.unipr.it

ABSTRACT

High-field reliability issues connected with hot electron and impact ionization are typically the reliability bottleneck of power FETs for microwave and millimeter-wave applications. This work deals with some aspects of this problem, from characterization and accelerated stressing techniques to the physical degradation mechanisms, using power AlGaAs/GaAs HFETs as a test vehicle.

INTRODUCTION

Microwave power amplification is a major industrial challenge, due to the exploding number of amplifiers required for wireless telecommunications portable units and base stations. Getting power outputs in the range of Watts or tens of Watts at C, X, and Ku bands and above with good efficiencies is a must for technologies competing in this market, like GaAs MESFETs, GaAs-based Pseudomorphic HEMTs (PHEMTs) and Heterostructure FETs (HFETs). In this respect, AlGaAs/GaAs HFETs (where a relatively low-doping AlGaAs Schottky layer is grown on top of a doped GaAs channel) show promising features.
Another vital concern for product success is of course reliability. Unfortunately, due to the hot electron and impact ionization conditions arising when large drain bias is applied, the power and reliability requisites conflict with each other. Burn-out casualties and gradual degradation phenomena were observed, with similar fetaures, in all of the FET technologies cited above. In particular, drain current reduction and DC and RF gain compression (*power slump*) seem to be the most frequent degradation modes fostered by high drain voltage conditions.
This work describes a case study of AlGaAs/GaAs power HFETs which were characterized and stressed with the aim of investigating the main aspects of their high-field degradation behavior.

DEVICES AND EXPERIMENTS

The devices under test (Fig. 1) are $Al_{0.25}Ga_{0.75}As$/GaAs power HFETs fabricated by Alenia Marconi Systems. They have a 200 µm gate width and length of 0.25 µm, and feature $I_{DSS} \approx 200$ mA/mm, $g_m \approx 150$ mS/mm, and $V_T \approx -2$ V. The off-state drain-gate breakdown voltage (BV_{DG}^{OFF}), measured at $I_G = -1$ mA/mm, is 19-20 V. At 10 GHz and 1-dB compression, the typical power density and gain are 0.6 W/mm and 9.6 dB.
Since the gate current is one of the main parameters characterizing the high-field regime (1), and both off-state (2) and on-state (3) breakdown are defined fixing a threshold for I_G, and since the drain-gate voltage (V_{DG}) is roughly proportional to the peak electric field between gate and drain, in order to study the influence of both I_G and V_{DG} on the degradation of the HFETs, we performed room temperature DC accelerated stress experiments under several bias conditions, as shown in Tab. I. In general, I_G and I_D were held constant during the stress.

RESULTS AND DISCUSSION

Fig. 2 shows the variation of the open-channel drain current (I_{DSS}, measured at V_{GS} = 0 V, V_{DS} = 2 V) during the hot-electron stress for the different bias conditions. The degradation approximately follows a square-law time dependence. Similar trends are observed for the transconductance degradation, and both ΔI_{DSS} and Δg_m are correlated with an increase of the drain resistance (R_D).The degradation varies dramatically with bias, even though the bias conditions are quite close to one another in the output plane. This points out to the need of a thorough bias-dependent assessment of the possible hot electron degradation effects.

As far as the relative influences of I_G and V_{DG} (which are not independent of one another) are concerned, the data of Fig. 2 indicate that both factors play a role: while larger I_G values lead to more severe I_{DSS} degradation, it is also true that for the same value of I_G, off-state stress conditions, where V_{DG} is larger, damage the HFETs more severely than on-state ones. In order to obtain a mathematical relationship linking the HFET degradation with I_G and V_{DG}, we established a failure criterion at $\Delta I_{DSS}/I_{DSS}$ = - 30% and extracted, for each device, the corresponding failure time (t_F). The set of failure time points can be interpolated with the following function:

$$t_F = A \left[|I_G| \left(V_{DG} - V_{DG}^{SAFE}\right) \right]^{-1/2}, \qquad (1)$$

where A = 30.4 h $(mA/mm)^{1/2}$ $V^{1/2}$, and V_{DG}^{SAFE} = 14.6 V. The fit is good, as shown in Fig. 3, and indicates a sort of threshold-activated V_{DG} acceleration. Eq. 1 is useful in that it allows to indicate a conservative safety limit for V_{DG} (V_{DG}^{SAFE}), in the proximity of which the failure time soars to infinity and the device behaves reliably. The parameters A and V_{DG}^{SAFE} are to be considered technology- and geometry-dependent, and should be extracted for a particular device lot through accelerated stressing.

A possible physical meaning can be attributed to Eq. 1 by making some very basic assumptions: (i) The degradation is proportional to the energy the carriers acquire between gate and drain, i.e., $\Delta I_{DSS}/I_{DSS} \propto E - E_{TH}$, where E_{TH} is a threshold energy for device damage, and $E - E_{TH} \propto V_{DG} - V_{DG}^{SAFE}$. (ii) $\Delta I_{DSS}/I_{DSS}$ is also proportional to the *number* of hot carriers which are responsible for the damage; therefore, assuming that the reverse I_G is a linear indicator of that, $\Delta I_{DSS}/I_{DSS} \propto |I_G|$. (iii) The degradation is proportional to the square of the stress time (as we said above, this is roughly true for the data of Fig. 2). From these assumptions follows Eq. 1.

As an aid for the physical interpretation of the experimental results, we have performed numerical simulations using a two-dimensional drift-diffusion commercial tool. A negative surface charge density of 2×10^{12} cm^{-2} was placed at the semiconductor-SiN interface on both sides of the gate in order to account for surface damage.

It is generally accepted that the main degradation mechanism triggered by high-field conditions in compound semiconductor FETs is the capture of electrons at the SiN interface over the gate-drain access region (4). This increases R_D and, consequently, leads to I_{DSS} degradation and *power slump*. An increase of R_D strictly correlated with the I_{DSS} and g_m degradation was indeed measured on our samples. Moreover, the enhanced surface state density on the gate side is confirmed by g_m frequency dispersion measurements. A temperature-dependent analysis allowed to attribute these traps an activation energy of about 0.5 eV.

In order to validate this Surface Charge Hypothesis (SCH), we compared the results of the simulation of standard (i.e., “before stress”) devices with those of the same HFETs where the negative surface charge density was raised to 3×10^{12} cm^{-2} between gate and drain (“after stress” simulations). The simulation results are shown and compared with measured ones in Fig. 4 and Fig. 5. The agreement between measurements and simulations indicates that the SCH can account for the experimental stress results.

CONCLUSIONS

When HFETs are biased under high-field conditions that degrade their characteristics, a strong bias dependence of the degradation exists, pointing out to the need of a careful bias-dependent reliability evaluation. Both the gate reverse current (I_G) and the drain-gate voltage (V_{DG}) should be considered as relevant accelerating factors. A fit to the experimental failure times revealed a thresold-activated V_{DG} dependence, and thus allowed to establish a well-defined safety limit for the drain-gate voltage. Numerical simulations have shown that the Surface Charge Hypothesis, whereby it is assumed that electrons are captured, during the hot-electron stress, at the interface between the device surface and the SiN passivation, can consistently account for the measured stress effects.

ACKNOWLEDGEMENTS

The author is grateful to all the colleagues involved in the HFET project: Claudio Canali, Domenico Dieci, Tiziana Tomasi (University of Modena and Reggio Emilia), and Giovanna Sozzi (University of Parma). Thanks are also due to Claudio Lanzieri and Antonio Cetronio (Alenia Marconi Systems). This work was supported by Consiglio Nazionale delle Ricerche through P.F. MADESS II, and by Ministero dell'Università e della Ricerca Scientifica e Tecnologica.

REFERENCES

(1) C. Canali, A. Neviani, C. Tedesco, E. Zanoni, A. Cetronio, and C. Lanzieri, "Dependence of ionization current on gate bias in GaAs MESFET's," 1993, *IEEE Trans. Electron Devices*, vol. 40, pp. 498-500.
(2) S. R. Bahl and J. A. del Alamo, "A new drain-current injection technique for the measurement of off-state breakdown voltage in FET's," 1993, *IEEE Trans. Electron Devices*, vol. 40, pp. 1558-1560.
(3) M. H. Somerville, R. Blanchard, J. A. del Alamo, G. Duh, and P. C. Chao, "A new gate current extraction technique for measurement of on-state breakdown voltage in HEMT's," 1998, *IEEE Electron Device Lett.*, vol. 19, pp. 405-407.
(4) R. Menozzi, "Hot electron effects and degradation of GaAs and InP HEMTs for microwave and millimeter-wave applications," 1998, *Semicon. Sci. Technol*., vol. 13, pp. 1053-1063.

Bias point	DUT	I_G [mA/mm]	I_D [mA/mm]	V_{DG} [V]
A	X8	- 0.1	8	14.84
A	X11	- 0.1	8	15.24
B	X2	- 0.1	2	17.16
B	X7	- 0.1	2	16.6
C	K4	- 0.25	8	16.3
C	W1	- 0.25	8	17.1
D	W8	- 0.25	16	16.4
E	K2	- 0.5	8	18.3
E	K3	- 0.5	8	17.1
E	K5	- 0.5	8	17.5
F	X5	- 0.5	0.5	20.1
F	X9	- 0.5	0.5	20.3
G	W7	- 0.05	8	14.68
H	W4	- 0.05	2	17
I	A10	- 0.1	15	14.7

Tab. I – Bias points used for the stress.

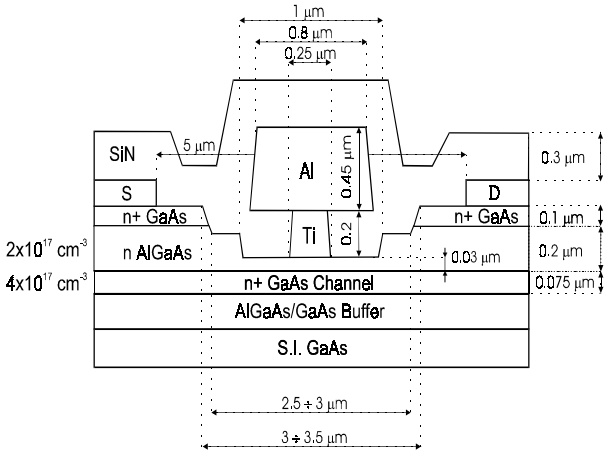

Fig. 1 – Schematic cross-section of the HFETs under test.

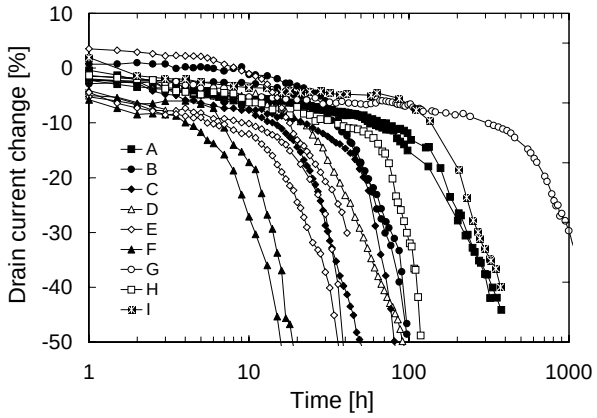

Fig. 2 – Drain current degradation for the stress points of Tab. I.

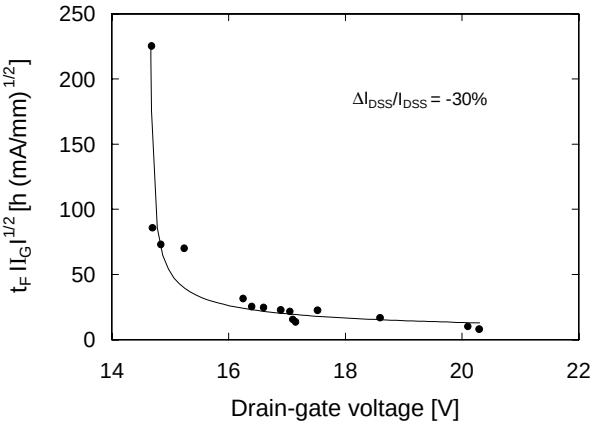

Fig. 3 – Experimental (points) failure times, multiplied by the square root of the stress gate current, vs. the stress drain-gate voltage. The interpolation given by Eq. 1 is also shown (line).

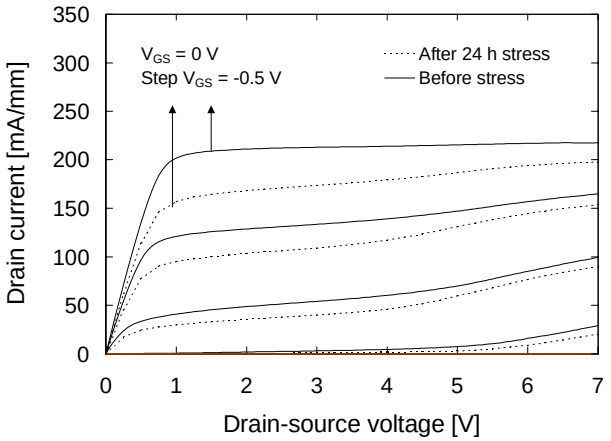

Fig. 4a – Measured output characteristics before and after a high-field stress.

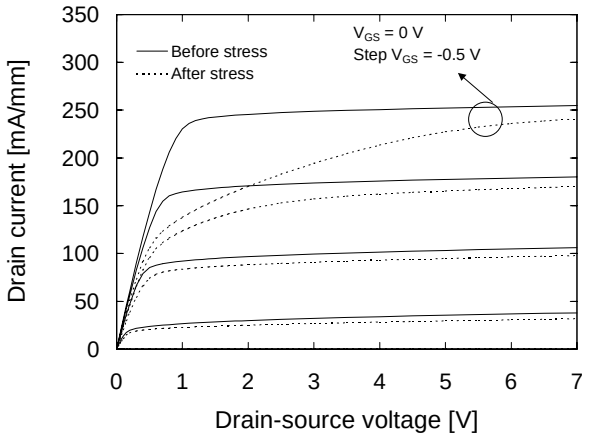

Fig. 4b – Simulated output characteristics before and after a high-field stress.

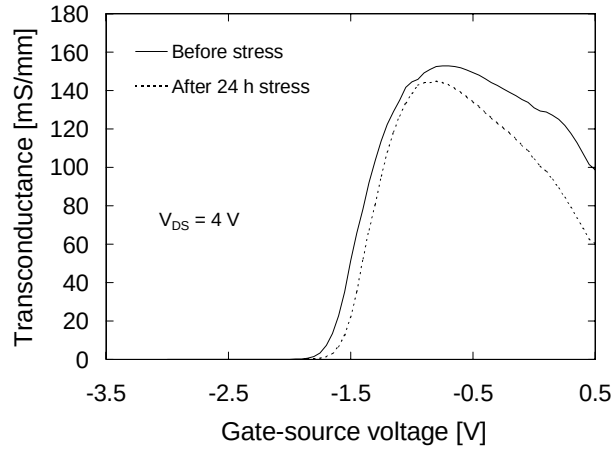

Fig. 5a – Measured transconductance before and after a high-field stress.

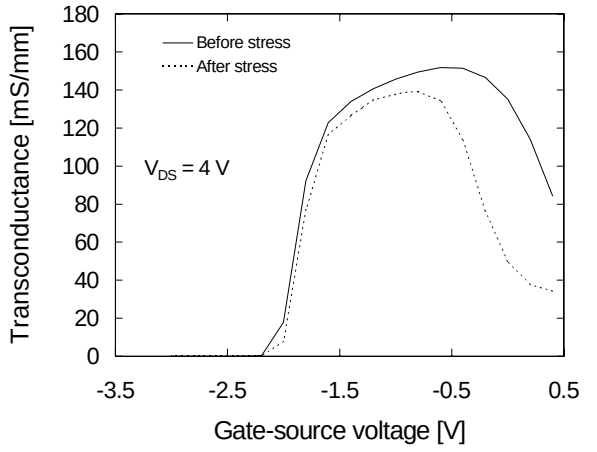

Fig. 5b - Simulated transconductance before and after a high-field stress.