Pulsed Electrical Stress Techniques for the Detection of Non-thermal Lifetime-Problems with Semiconductor Devices and their IC's

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ABSTRACT

A method is presented for the investigation of non-thermal generated defect mechanisms with semiconductor devices. This method bases on applying Transmission Line Pulses (TLP) to the device to generate lifetime limiting defects. The pulse length is chosen down to 20 ns. This is short compared to the thermal time constant of the respective devices providing the generation of non-thermal defect mechanisms. Significantly higher current densities are used in comparison with normal operation to shorten the time of electrical defect generation. Current and voltage of the impulse response, subsequent DC I/V and noise measurements are used to characterize the occurring defect mechanisms. Pulsed electrical stress techniques are proposed for different III/V semiconductor devices (e.g. TLM-structures, HBT) and results obtained with this method are presented.

INTRODUCTION

Increased lifetime and reliability is a major issue in manufacturing III/V-semiconductor devices since more complex IC's are employed in large-scale production. On-wafer measurements are used for fast monitoring of device and circuit reliability. Reliability studies for semiconductor devices are done in the majority of cases using accelerated lifetime testing approaches. Most of those use increased temperature and DC-level as stress factors to accelerate current and temperature driven defect mechanisms to shorten the measurement duration [1]. The Arrhenius law is used to calculate activation energies of the degradation mechanisms. Mainly, thermal degradation mechanisms are generated by this procedure because the devices are significantly heated. On that account, this technique is not appropriate for the detection of non-thermally induced defect generation mechanisms.
For this reason, a method has been developed using electrical pulses with a pulse length that is significantly shorter than the thermal time constant of the respective device but therefore increased current density [2]. These high current densities allow well-defined electrical stress of single semiconductor layers or interfaces without excessive heating of the whole device. The pulse width is set according to the thermal time constant of the device (minimum pulse length: t_{min}=20 ns). The current densities applied to the device are adjusted by varying the open-source voltage of the pulse generator. The influence of the pulse width, the pulse voltage and the number of pulses is analyzed. Information on the physical processes is obtained by this method, which are behind the lifetime limitations but activation energies are not directly derived yet. Knowing these, a more precise lifetime estimate can be expected since the reason for given activation energies is more clearly understood. Defect mechanisms are investigated using the real-time voltage and current impulse response, DC I/V and noise measurements [3-5]. In the following, methods and results are presented for TLM-structures representing one-port devices and HBT representing two-port devices.

NON-THERMAL PULSED STRESS TECHNIQUES FOR SEMICONDUCTOR DEVICES

Generally, pulsed stress techniques can be applied to all kind of semiconductor devices and their respective integrated circuits. There are two main approaches for a well-directed generation of defect mechanisms. In the first approach pulses are applied to the device under normal operating conditions, which is the preferable method for one-port devices. The second approach is based on the generation of defect mechanisms only at a certain interface to judge device quality, which is the preferable method for two-port devices or integrated circuits. In this case, the device is not operated under normal conditions but under conditions which are suitable for the enhanced generation of defects at a certain interface. This is why diverse devices require different measurement set-ups. The general approach of application of non-thermal pulsed stress techniques to semiconductor devices is divided into the following four steps:

1. The extraction of thermal characterization data for the device or the different interfaces of one device.
2. The detection of the threshold voltage for the device or the different interfaces of one device.
3. The analysis of relevant defect generation mechanisms.
4. The well-defined excitation of defect mechanisms using the TLP-method.

In the next section, results are presented, which are achieved using the TLP-method for TLM-structures and HBT following the given approach.

1) The extraction of thermal characterization data for the device or the different interfaces of one device:
Thermal time constant are determined for the base-, collector- and emitter TLM-structures of different devices to $\tau_{thermal}$=40...50 µs and for HBT to $\tau_{thermal}$=1.8 µs. Figure 1a) and figure1b) show the voltage response of a TLM-structure and a HBT with the influence of electro-thermal coupling.

2) The detection of the threshold voltage for the device or the different interfaces of HBT:
At first, TLM-structures are investigated representing the base-, the collector- and the emitter-layer of HBT. The pulse response of a TLM-structure is shown in Figure 2a). A strong drift in the voltage response is measured for an open circuit pulse amplitude of 38 V, which reflects a beginning instability in large-signal sample characteristics. When the pulse amplitude is increased to 40 V, reversible sample breakdown can be extracted either from the voltage or from the current response. The voltage response in Figure 2a) shows a sudden transient increase during the square pulse for this level because of current saturation. Therefore, the sample current decreases at the same time point. For a further increase of the pulse amplitude to 46 V, a higher instability is found, which leads to a non-reversible degradation of the sample. Only a slight increase in the sample resistance (+10%) is found for the maximum pulse amplitude of 51 V as is shown in figure 2b). For an amplitude of 46 V (which already causes the strong distortion in pulse response visible in Figure 2a)), the variation is still within the measurement-error tolerance range. For a pulse amplitude of 40 V on the other hand, no visible degradation is found in the IV-characteristics although the voltage response measurement already reflects a clear instability for this voltage level. Similar response measurements have been conducted for TLM with a contact spacing of w= 6 ...60 µm for base, emitter and collector layers.
Next, the threshold is investigated for the base-emitter (B-E) and the collector-emitter (C-E) interface of the process-control-monitor (PCM) HBT using pulses with the pulse width of τ_{pulse}=50 ns. The collector is kept floating when pulses are applied to the C-E interface and the base is kept floating when pulses are applied to the C-E interface. In the following, pulses are applied to the B-E interface. According to this approach, most of the electrons drift from the emitter through the base into the collector. The diffusion length is approximately 1.7 µm for a p-type GaAs with a doping density of $N_D = 10^{19}$ cm^{-3} , an electron lifetime of $\tau_n = 10^{-9}$s and a diffusivity of D_n = 30 cm^2/s [6]. This is longer than the base-width which is around 100 nm. Electrons are not extracted in the collector as it remains floating. Therefore, the number of charge carriers in the base rises above the level of normal operation. Thus, the recombination in the base is enforced. Electrons have high energies while drifting from the emitter through the base into the collector during their movement through the device. So the electrons have these high energies while passing the most sensible parts of a HBT: the junctions, especially the heterojunction. This stress is equivalent to the stress under normal operating conditions. The B-E interface was found to be the most critical part [1] because a degradation is observed for smaller voltages. A first degradation effect can be observed for a device-specific voltage at the B-E interface increasing the base-emitter stress. An additional degradation is detected at the B-C interface by further increase of the stress. The degradation of the interfaces is gradually increased with increasing stress until the breakdown of the device is detected. As the current is fed into the base-emitter diode of the HBT, one would expect only this junction to degrade by the stress. Measurements show instead that the B-C diode characteristic of the devices changed. Figure 3b) shows the degradation of a PCM HBT after B-E stress. Finally, the degradation threshold of the respective RF-HBT is extracted.

3) The analysis of relevant defect generation mechanisms:
The relevant defect mechanisms for TLM-structures are field-related mechanisms including electromigration and lateral material transport mechanisms [7]. Such a material transport is shown in figure 3a) for a collector TLM structure, which was stressed by a sequence of electrical pulses until the first degradation was detected in the IV-measurements.
Relevant defect mechanisms and the influence of leakage currents on reliability issues in connection with HBT are discussed in [8-10]. It is assumed that only one defect mechanism is responsible for the degradation of both diodes. This is called Recombination Enhanced Defect Reaction (REDR) mechanism, which is explained in Ref. [1]. The base leakage current is caused by recombination centers in the base. Some of the recombination at these centers releases energy directly to the lattice defect and most likely additional defects are generated. The base current increases as the number of charge carriers in the base rises above the level of normal operation. Thus, the recombination in the base and the corresponding REDR effect is enforced. It is proposed here that the defect mechanisms observed at interfaces are dependent on the material quality. This proposal need to be verified still by further work.

4) The well-defined excitation of defect mechanisms using the TLP-method:
After the determination of the degradation threshold, the pulse amplitude is set to a value below this threshold to generate a certain current density (J=100 kA/cm^2 ... 400 kA/cm^2). The pulse number for each run is increased to N_p=[100 ... 100000] at the same time. Characteristic values are extracted, such as the current gain of the HBT or the ideality factors of the diodes and are plotted versus the pulse number. In the following, different single-finger HBT are

investigated with an emitter area of $S_{Emitter}$= 50 µm^2 ... 90 µm^2. Figure 4b) shows the normalized current gain of two different devices with different stress current densities. For device “B”, two degradation effects take effect: The first effect occurs early during the measurement and decreases the gain rapidly but can only be seen at low base currents (I_{BE} < 10µA) because the B-E diode exhibits a high leakage current in this range as it is shown in Figure 4a) (curve: 50000 pulses with 10 V). This effect is not representative for normal operation conditions, but it is a sensible diagnostic tool for the detection of defects in the interfaces. The decrease of current gain indicates leakage currents caused by recombination centers in the base-emitter junction. After this first breakdown of the gain, the device is stable over a high number of pulses and shows even an increase in gain as known for the burn-in effect due to hydrogen compensation. After a number of pulses - characteristic for a device - a slow degradation of the gain can be observed that leads finally to a total failure. Device “A” withstands the stress without any indication of leakage currents. The only effect observable is a strong increase in current gain due to hydrogen compensation [1] as it has been reported in conventional lifetime test for carbon-doped HBT [12]. Comparing the curves for the different devices in Figure 4b), it is evident that device “A” is less sensitive to current induced degradation mechanisms than device “B”.

CONCLUSION AND OUTLOOK

Pulsed electrical stress techniques for the detection of non-thermal defect mechanisms are presented. Results for TLM-structures and HBT degraded by pulsed electrical stress are shown excluding thermal effects. It has been shown that pulsed electrical stress techniques allow a fast characterization of reliability-relevant properties and of defect generation mechanisms related to III-V semiconductor devices. Further investigations will compare the achieved results with those of conventional lifetime prediction methods. Relevant defect mechanisms will be identified and a parameter equivalent to the Arrhenius activation energy will be derived. Further work is in progress to obtain useful information on lifetime prediction with the pulsed measurement results.

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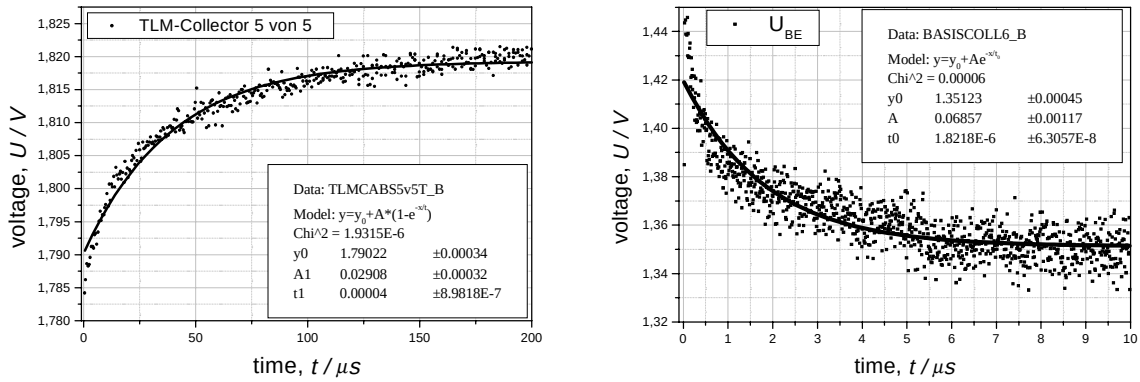
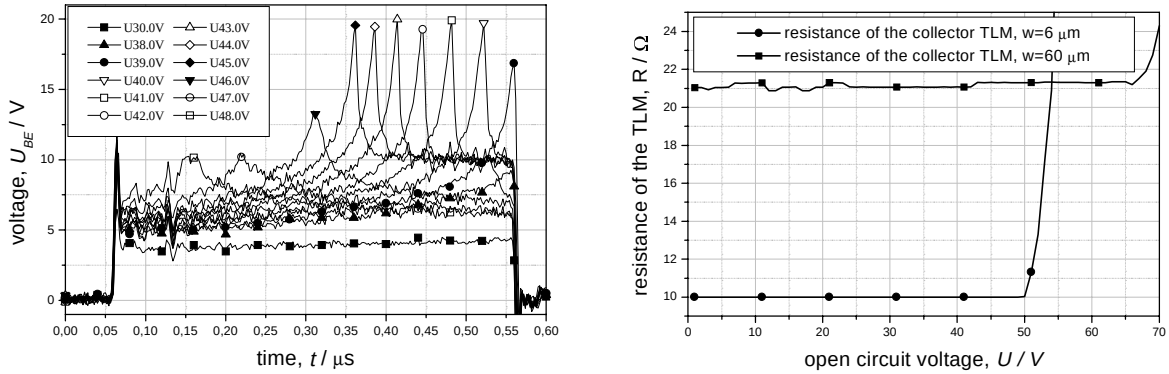


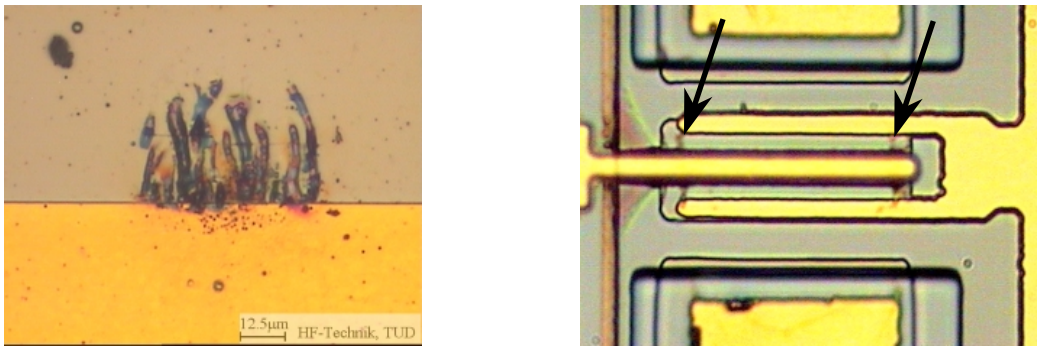
a) **b)**

Figure 1: a) Measured voltage response of a TLM-collector structure with w=6 µm spacing. b) Measured voltage response of a HBT under normal operation conditions.



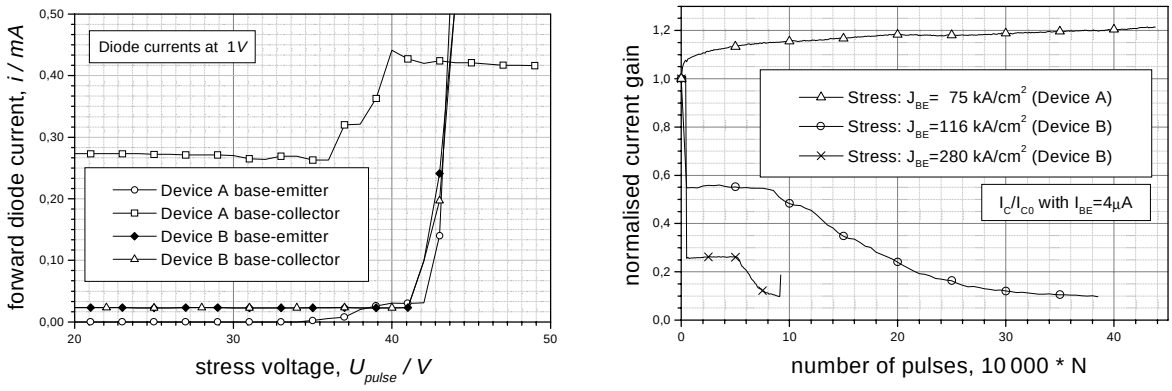
a) **b)**

Figure 2: a) On-wafer pulse voltage response measurement for a collector TLM structure (w=6 µm) for different open circuit pulse voltages. b) Degradation resistance of collector TLM structures with w=6 µm and w=60 µm over the applied pulse voltage.



a) **b)**

Figure 3: a) Degradation of a collector TLM structure (w=60 µm) stressed by pulses with increasing pulse amplitude due to electromigration. b) Degradation of a PCM test HBT after B-E forward stress, 100ns pulse, I=0.45 A.



a) **b)**

Figure 4: a) Base-emitter and base-collector currents for different HBT. b) Normalized current gain over the number of applied pulses for different HBT