Submicron lateral scaling of HBTs and other vertical-transport devices: towards THz bandwidths

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Abstract— **With appropriate device structures, combined lithographic and epitaxial scaling of HBTs, RTDs and Schottky diodes results in rapid increases in device bandwidths. 0.1 μm InGaAs RTDs have oscillated at 650 GHz, Submicron heterojunction bipolar transistors (HBTs) fabricated with substrate transfer processes have obtained 21 dB unilateral power gain at 100 GHz; if extrapolated at -20 dB/decade, this corresponds to a 1.1 THz power-gain cutoff frequency. HBT current-gain cutoff frequencies as high as 300 GHz have been obtained.**

I. Introduction

DEVICE scaling –reduction of layer thicknesses and lithographic feature sizes – is central to high frequency semiconductor device design. As CMOS gate lengths have been reduced, clock rates have progressively increased. 0.13 μm Si MOSFETs exhibit ~70 GHz f_τ. Compared to silicon, III-V compound semiconductors offer higher electron mobilities, higher electron saturation drift velocities, and stronger heterojunctions, hence III-V semiconductor devices can obtain higher bandwidths than their silicon counterparts. Yet III-V devices must be aggressively scaled to deep submicron dimensions if they are to remain competitive with silicon.

III-V heterojunction bipolar transistors (HBTs), in particular, have not been adequately scaled. GaAs- and InP- based HBTs are typically fabricated at 1–2 μm minimum feature sizes and operate at 1–2 $\times 10^5$ A/cm^2. This is in marked contrast to both III-V HEMTs, where 0.1 μm gate lengths are typical, and Si/SiGe HBTs, where emitter widths are 0.1 μm [1] and emitter current densities are as high at 10^6 A/cm^2. Because of this aggressive scaling, Si/SiGe HBTs are a major competitive threat to III-V HBTs. Addressing this, we have developed InAlAs/InGaAs HBTs with submicron emitter and collector dimensions, and have obtained 1 THz (*extrapolated*) power-gain cutoff frequencies (f_{max}) and 300 GHz current-gain cutoff frequencies (f_τ). Challenges in HBT submicron scaling include collector definition, emitter parasitic resistance, and support of high collector current densities.

Scaling laws and scaling examples

We will develop HBT scaling laws by first considering high frequency diodes. Dominant time constants for Schottky diodes are shown in fig. 1. The device has a junction impedance $R_j = kT/qI$, a depletion capacitance C and a parasitic series resistance R_s arising from the bulk resistivity of the buried N+ layer and its Ohmic contacts. Given junction depth D, there is a transit time $\tau_{\text{transit}} \propto D/v_{\text{electron}}$. Given junction width W, there is capacitance $C \propto WL/D$. Given device stripe length L, the buried layer & bottom contact resistance R_s varies as $1/L$.

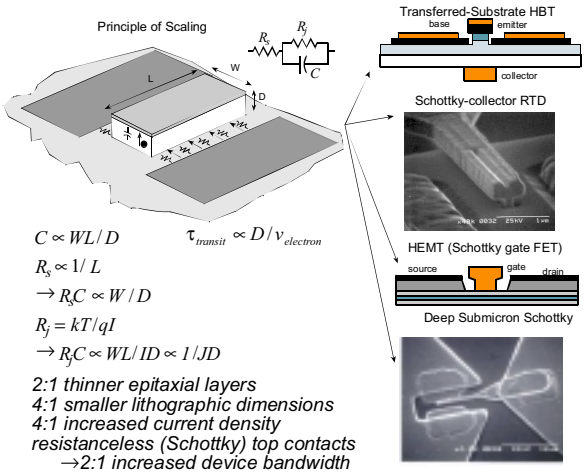

Fig. 1. Scaling laws for high-frequency devices

We wish to double the device bandwidth. This requires thinning the depletion layer 2:1 to proportionally reduce τ_{transit}. In reducing D 2:1 with W left unchanged, we have doubled the device capacitance, doubling R_sC. Our intent is instead to *decrease* R_sC by 2:1; to do this we must now decrease the contact stripe width W by 4:1. With this combined scaling, C has now been reduced to 1/2 its original value. If the current I is left unchanged, the time constant $R_jC = (kT/qI) \cdot C$ is thus also reduced by the desired 2:1 ratio. Note that the device junction area WL has been reduced 4:1; the device current density has thus been increased fourfold.

These are the scaling laws for Schottky mixer diodes. Each desired 2:1 increase in device bandwidth requires a 2:1 reduction in epitaxial layer thicknesses, a 4:1 decrease in junction width (lithographic scaling), and a 4:1 increase in operating current density.

Exploiting such scaling, Siegel *et al* have reported submicron Schottky mixers diodes with low noise at 2.5 THz [3], [4]. Figure 2 shows a 0.1 μm $\times$0.5 μm T-gate Schottky diode (with 150 Å depletion thickness) used for submillimeter-wave harmonic mixing [2].

Unlike Schottky diodes, PN diodes have both anode

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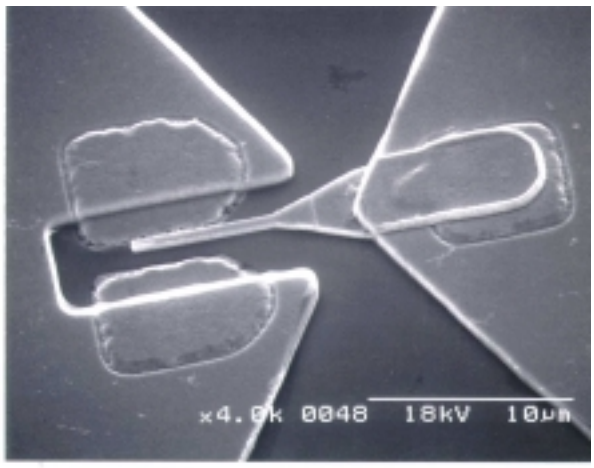

Fig. 2. Submicron (0.1μm $\times 0.5\mu$m) Schottky mixer diode with 150 Å depletion depth. Calculated RC and transit-time cutoff frequencies are $\sim 15THz$.

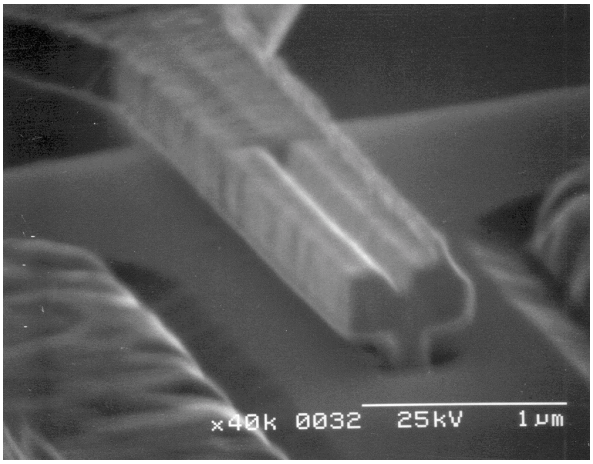

Fig. 3. 0.1 μm InGaAs/AlAs Schottky-collector RTD.

(top) and cathode Ohmic contacts. The top contact has resistance $R_{\rm top} = \rho_{\rm contact}/LW$, resulting in a time constant $R_{\rm top}C \propto \rho_{\rm contact}/D$. Since a 2:1 desired improvement in device speed required a 2:1 reduction, in D (for reduced transit time), the required 2:1 reduction on $R_{\rm top}C$ requires a 4:1 improvement in $\rho_{\rm contact}$. Devices with top Ohmic contacts can be very difficult to scale: each 2:1 improvement in device speed requires a 4:1 improvement in contact resistivity.

Lack of minority carrier storage is an often-cited speed advantage of Schottky diodes over their P-N counterparts; elimination of the top Ohmic contact is an advantage of equal significance. Zero gate contact resistance is a crucial advantage of the (Schottky-gate) MESFET / HEMT [5] over the JFET; in the JFET, gate Ohmic contact resistance increases as the gate length is reduced.

II. Schottky-collector RTDs

A resonant-tunnel diode (RTD) has an equivalent circuit similar to that of the Schottky diode shown in fig. 1. The device has a negative resistance R_n replacing R_j of the Schottky diode, plus series resistance $R_{\rm total} = R_s + R_{\rm top}$ and depletion capacitance C. R_n varies as $1/I_{peak}$, the peak tunneling current density. If the electron storage time in the quantum well τ_{qw} is negligible, the device maximum oscillation frequency is $f_{max} = (1/2\pi C)(R_n R_{\rm total})^{-1/2}$; if τ_{qw} is dominant, $f_{max} = (1/2\pi)(R_n R_{\rm total})^{-1/4} C^{-1/2} \tau_{qw}^{-1/2}$.

RTD scaling follows the rules above. Current densities must be high. Depletion layers must be thin to avoid high transit times. Lithographic scaling reduces the R_sC time constant. If the RTD has a top Ohmic contact, then reduction of $R_{\rm top}C$ to values necessary for submillimeter-wave oscillation requires very low contact resistance, and InAs contacts [6] are then employed. Yet, the RTD top Ohmic contact is unnecessary, and can be replaced by a direct Schottky contact to the *fully-depleted* electron drift layer, thereby eliminating $R_{\rm top}$. An RTD with a 0.1 μm T-gate Schottky contact, 350 Å depletion thickness, and $5 \cdot 10^5$ A/cm^2 current density (fig. 3) has a estimated (but not measured) 2 THz f_{max}. 64-element monolithic arrays of Schottky-collector RTDs have oscillated at 650 GHz (fig 4) [2].

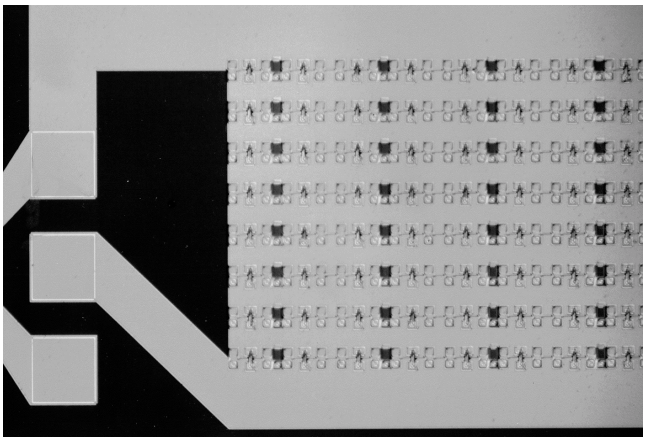

Fig. 4. A 64-element, 650 GHz, RTD quasi-optical array oscillator.

III. HBT scaling

An HBT is a pair of coupled diodes, and follows scaling laws similar to the Schottky diode. A 2:1 desired improvement in HBT bandwidth requires 2:1 reduction in base and collector transit times, requiring a $\sqrt{2}$:1 reduction in the base and a 2:1 reduction in the collector epitaxial layer thicknesses. For a 2:1 improvement of *all* HBT RC and delay terms, the emitter-base and collector-base junction widths (lithographic feature size) must also be reduced 4:1, the collector current density increased 4:1, and the emitter Ohmic contact improved 4:1.

A. Transferred-Substrate HBTs

An immediate difficulty is the required reduction in the collector junction width. In mesa HBTs the collector-base junction must lie under both the emitter stripe and under the base Ohmic contacts, which must

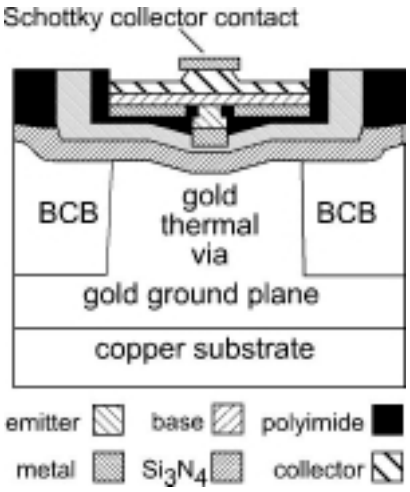

Fig. 5. Schematic cross-section of a transferred-substrate HBT

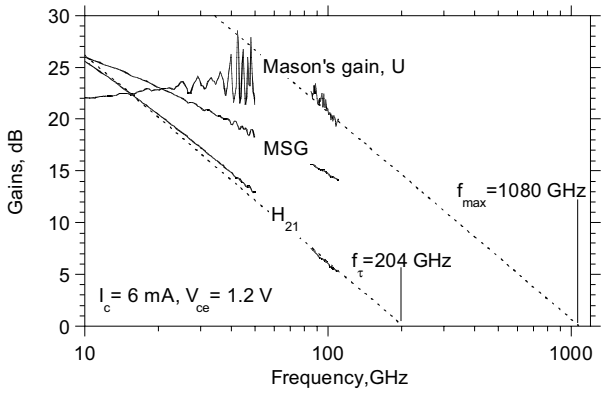

Fig. 7. Gains of a 0.4 μm × 6 μm emitter and 0.7 μm × 10 μm collector HBT fabricated using electron-beam lithography. Theoretical -20 dB/decade (H_{21}, U) gain slopes are indicated. The device exhibits an *extrapolated* 1.08 THz f_{max}

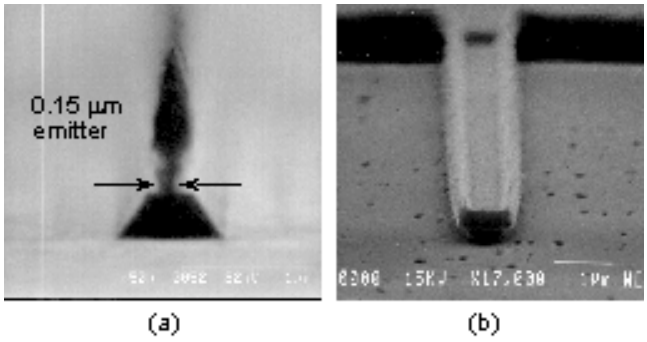

Fig. 6. E-beam HBT: test structure with 0.15 μm emitter-base junction (a), and 0.4 μm Schottky collector stripe (b)

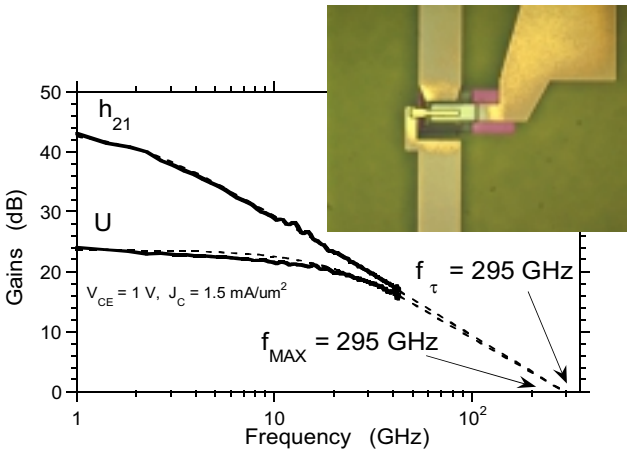

Fig. 8. Measured RF gains for an HBT with a 300 Å base with 52 meV grading and a 2000 Å collector.

be a minimum width of one contact transfer length, typically ~ 0.25 μm. A minimum collector-base junction width is thus defined, and a lower limit is set for HBT scaling

Using substrate transfer processes [7], HBTs can be defined with emitter-base and collector-base junctions on opposing sides of the base epitaxial layer (fig. 5). The minimum collector junction width is now determined by the emitter width alone, and need not include the widths of the base Ohmic contacts; collector junctions can be scaled to submicron dimensions. Submicron InAlAs/InGaAs devices fabricated using electron-beam lithography (fig 5) exhibit 21 dB unilateral power gain at 100 GHz (fig. 7). Extrapolation at -20 dB/decade (to be treated with caution) suggests an 1100 GHz f_{max}. In addressing limits to collector scaling, one alternative to substrate transfer is an undercut collector-base junction [8]. A second alternative is very high (carbon) base doping within a normal mesa HBT structure – at $\sim 2 \cdot 10^{20}/\mathrm{cm}^3$ base doping, the contact transfer length is $\sim 0.1\mu$m, and very narrow base mesas can then be employed.

The HBT of fig. 7 has narrow emitter and collector junctions but thick 400 Å base and 3000 Å collector layers, and hence has high f_{max} but only 200 GHz f_τ. While such a device will provide high gains in tuned millimeter-wave amplifiers, more general circuits require simultaneously high values for f_τ and f_{max}. Digital circuits, in turn, have gate delays in which $(\tau_b + \tau_c)$, $C_{bc}\Delta V_{\mathrm{logic}}/I_c$, $R_{bb}C_{je}$, $R_{ex}C_{je}$ and $R_F bb(\tau_b + \tau_c)I_c/\Delta V_{\mathrm{logic}}$ are all significant terms.

To ensure a 2:1 improvement in *all circuits* employing the HBT, all HBT transit times and RC time constants must be reduced 2:1. In addition to lithographic scaling of emitter and collector junction widths–as demonstrated in the high-$f_{\max}$ devices–epitaxial layer thicknesses, emitter contact resistance, and emitter current density then must also be scaled by the proportions given earlier. Figure 8 shows measured RF gains for a developed in our efforts to realize logic gates at 70-100 GHz clock rates. Simultaneous 295 GHz f_τ and f_{max} are obtained.

Circuit results in the substrate transfer process include DC-80 GHz lumped and distributed amplifiers [10], 66 GHz true static frequency dividers [11],

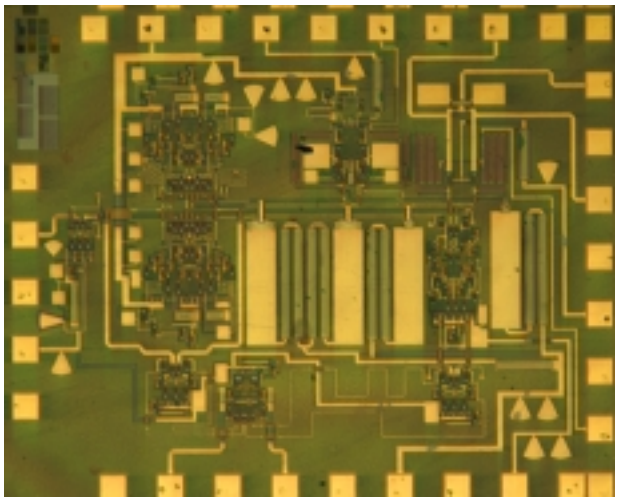

Fig. 9. 20 GHz-clock-rate Δ-Σ ADC in the transferred-substrate process.

W-band medium-power amplifiers, and 20-GHz-clock delta-sigma analog-digital converters [12].

IV. Conclusions

With bipolar transistors, improved bandwidths are obtained by vertical scaling (thinner base and collector layers), combined with lateral scaling (narrower collector and emitter junctions), increased current density, and progressive improvements in emitter Ohmic contacts.

Substrate transfer processes facilitate lateral scaling; remaining difficulties include the emitter contact resistivity, loss of breakdown in thin collector layers, and reliability and heatsinking under high-current-density operation.

While III-V HBTs benefit from strong heterojunctions, high mobilities, and high electron velocities, Si/SiGe bipolar transistors have been much more aggressively scaled. Aggressive submicron scaling of III-V HBTs can result in THz device bandwidths.

Acknowledgments

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