0.3µm-N-HIGFET CAPABILITIES FOR MICROWAVE POWER APPLICATIONS

M. ***TOUIRAT****, M.* ***ROGER****, L. T.* ***NUYEN****, Y.* ***CROSNIER****, and G.* ***SALMER***

Institut d'Electronique et de Microélectronique du Nord (**IEMN**), Avenue Poincaré, B.P. 69, 59652 Villeneuve d'Ascq cedex, France, UMR CNRS 8520, e-mail : miloud.touirat@iemn.univ-lille1.fr

*** PICOGIGA**, 5 Rue de la Réunion, Z. A. De Courtaboeuf, 91940 Les Ulis, FRANCE

ABSTRACT

0.3µm HIGFET transistors have been realized for microwave power applications. Power measurements at 3.5GHz using load-pull testbench have been carried out. Transistors exhibit an output saturated power of 16dBm and a power density of 370mW/mm for a 3V drain-to-source voltage.

INTRODUCTION

Complementary GaAlAs/GaInAs/GaAs Heterostructure Insulated-Gate Field-Effect-Transistor (C-HIGFET) offers the prospect of high speed and low power dissipation IC's [1], [2]. Moreover, N-HIGFET is a good candidate for new microwave power applications (wireless) thanks to his low supply voltage (less than 4V) and his good linearity performance [3].

Indeed, HIGFET heterostructure includes an undoped supply layer and its behavior is characterized by an enhancement mode charge control law. This allows two main interesting features:

-First, the gate-source control voltage Vgs is positive and then only one DC bias source is needed

-Secondly, a good linear command can be expected in a wide Vgs interval. Moreover, the HIGFET undoped heterostructure combined with an appropriate implantation process allows to obtain high breakdown voltage, and reduced parasitic DX trap levels in the channel. In this paper, N-HIGFET fabrication process and typical power device results are presented.

DEVICE FABRICATION

The HIGFET structure is grown on a 2-inch semi-insulating GaAs substrate by molecular beam epitaxy. It consists of a pseudomorphic $Ga_{0.25}Al_{0.75}As/Ga_{0.8}In_{0.2}As/GaAs$ heterostructure with an undoped channel, described in Fig. 1. The main steps of sidewall technology are refractory gate definition, first implantation self-aligned to the gate, sidewalls definition, second implantation self-aligned to the sidewalls and ohmic contact evaporation [4].

To reduce short channel effect, Si implantation consists of 1×10^{13}at/cm^2 for the first and 10^{15}at/cm^2 for the second. In Fig. 2, cross section SEM photography of the resulting structure is presented.

Gold is deposited on the gate in order to reduce its parasitic resistance. Typical distance between drain and source contacts Lsd is 1.8µm. Interconnect metallization is made by Ti/Au. Device is finally passivated with Si_3N_4.

DC AND AC RESULTS

Typical I-V characteristics of 2×50×0.3µm^2 (number of fingers×gate width×gate length) N-channel are shown in Fig. 3. High values of drain-to-source current density and transconductance are obtained: 460mA/mm at Vds=Vgs=2V and 480mS/mm at Vds=2V and Vgs=1.2V, respectively. Variations of transconductance and current versus Vgs are represented in fig. 4.

Gate thickening makes it possible to reduce greatly its parasitic resistance: for a 0.3µm gate length, thickening allows to obtain 0.2kΩ/mm instead of 6kΩ/mm. This improves the dynamic performance of the device, in term of maximum oscillation frequency (Fmax) and maximum available gain (MAG). Fmax increases from 31GHz to 55GHz and MAG at 10GHz from 10dB to 15dB for typical DC bias conditions: Vgs=1.2V and Vds=2.5V.

In addition, the gate turn-on-voltage is 1.6V (Vgs @ Igs = 1µA/µm). The threshold voltage Vth is 0.4V and its standard deviation on a 2-in wafer is equal to 60mV. To increase the current excursion for power applications, it is possible to reduce Vth close to zero volt by increasing the Si doped beneath the channel.

POWER RESULTS

Discrete HIGFET samples have been studied by measuring their Output Power (Pout) and Power Added Efficiency (PAE) at 3.5GHz using a Load Pull testbench which permits to realize input and output matching. A class AB biasing regime has been considered. Fig. 5 shows load-pull power performances at 3.5GHz for very low supply voltages:

At Vds=2.5V, the output saturated power was 15dBm, the power density was 290mW/mm, and the corresponding gain was 16dB. At Vds=3V, the output saturated power reach 16dBm, the power density is 370mW/mm, and the corresponding gain is 17dB. **This is the first power results for a 0.3µm gate length HIGFET made at 3.5GHz.**

Moreover, the 1dB compression output power reach about 155mW/mm and the maximum power added efficiency is 50% for the two DC bias values. These results are quite interesting compared, for example, to a power density of 270mW/mm and a linear gain of 7dB obtained for a 0.25µm-DC-HFET [5] at high supply voltage.

CONCLUSION

Preliminary investigations of HIGFET transistors for power applications show very promising performance at 3.5GHz. At 3.5GHz, a 0.3µm-N-type HIGFET exhibited a linear regime power gain of 15dB, an output power density of 290mW/mm with an associated PAE of 50%, **at a DC bias of 2.5V.**

To complete the study, intermodulation measurement are performed to see the linearity of the HIGFET Heterostructure for high power applications. An intermodulation measurement at 10GHz, with tone 1MHz apart, is performed for this device. The Third Order Intercept (TOI) points reach a value of 13.6dBm, for a gate width of 100µm.

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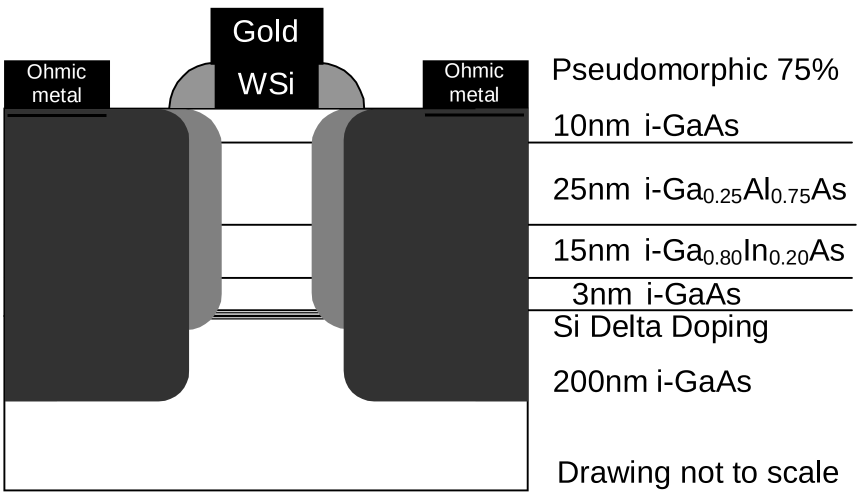

Fig. 1 : Cross-section of pseudomorphic HIGFET epitaxy

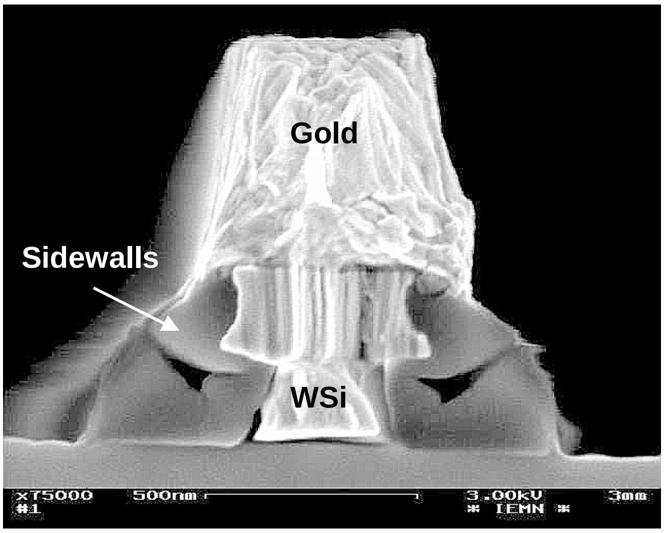

Fig. 2 : SEM photography of a 0.3µm WSi/Au gate with SiO_2 sidewalls.

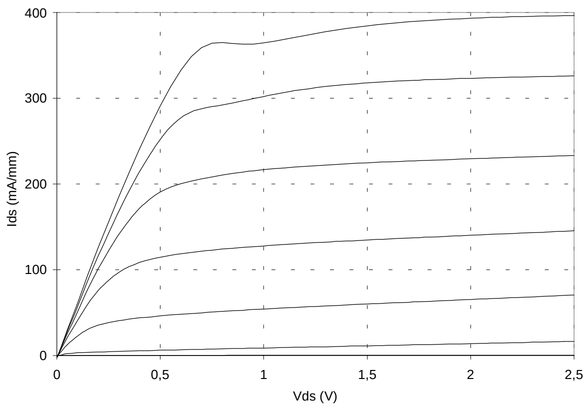

Fig. 3 : Id-Vds measurements of 0.3µm-N-HIGFET. Vgs max = 1.6 V. Step Vgs = 0.2 V.

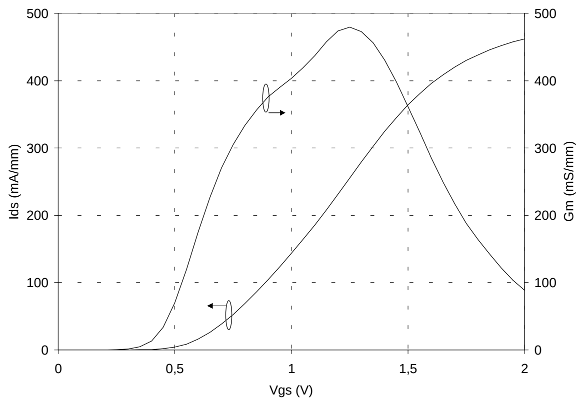

Fig. 4 : Variations of transconductance and current versus Vgs for a 2×50×0.3µm^2 at 2V.

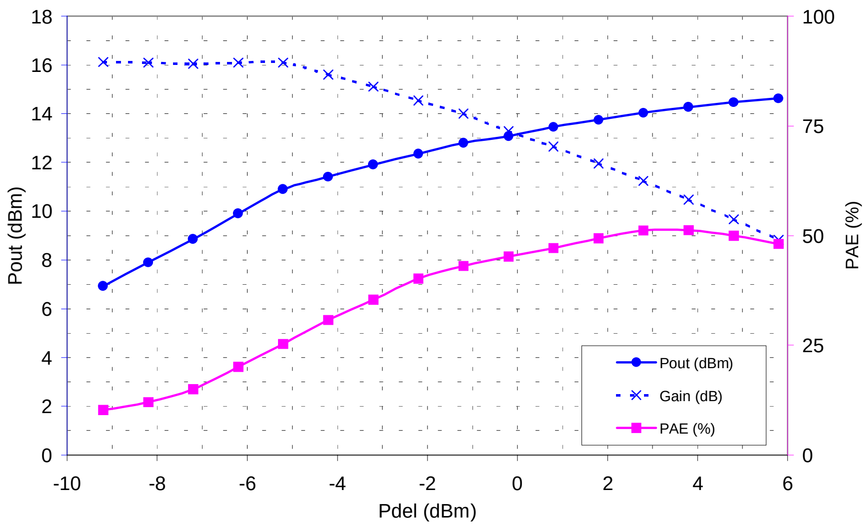

Fig. 5 Output power, PAE and gain dependence upon input power for an 2×50×0.3µm^2 at 3.5GHz and 2.5V.