High efficiency LOW AM/PM 6W C-band MMIC power amplifier for a space radar program

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Abstract - **This paper describes the design of a compact C-band MMIC power amplifier. Intensive non-linear and electro-magnetic simulations with accurate table-based models allowed the chips to achieve very good performance. A linear gain of 28 dB, an output power greater than 6 W with 50 % of power added efficiency and 3°/dB of AM/PM conversion at 2.5 dB gain compression have been measured over production at ambient temperature in the useful bandwidth.**

I. INTRODUCTION

New developments of active antennas for satellite synthetic aperture radar (SAR) applications require high output power and high power added efficiency amplifiers. Due to the large amount of T/R modules having to be integrated, a full MMIC output power amplifier is a very interesting solution in order to reduce the size and the weight of the equipment. Then, improving the MMIC amplifier PAE state of art is a mandatory challenge in order to compete with hybrid solutions because payload consumption is a critical parameter. In the same time, SAR applications require two other important characteristics : to insure MMIC unconditional stability under pulsed drain bias conditions and to reduce AM/PM conversion in order to reach phase stability and linearity requirements.

II. MMIC DESIGN

Devices modeling :

The amplifier has been designed using Triquint-Texas 0.25 µm power P-HEMT process.

A full pulsed S-parameter characterization (from DC to 40 GHz) of transistors issued from previous runs [1] was performed to extract the linear and non-linear models. A customized table-based model [2] including the main current source $I_{DS}(V_{DS},V_{GS})$ and the capacitance's $C_{GS}(V_{DS},V_{GS})$ and $C_{GD}(V_{DS},V_{GS})$ has been computed to insure the accuracy of simulations even under deep compression levels.

Circuit description :

As shown on figure 1, this 2 stages amplifier is constituted of a 4x1.5 mm stage driving a 8x2 mm power stage. They are both biased in deep AB class (I_{MAX}/10) in order to maximize PAE. A 2.7:1 ratio in gate developments between the two stages guaranties the linearity of the 1st stage within the deep global compression level of the complete circuit and makes the inter-stage power matching easier. The final dimension of the chip is 5.2x3.5 mm².

The output power and the power added efficiency have been optimized using load-pull and source-pull simulations. The inter-stage was also optimized considering losses, gain flatness and power matching of the first stage.

The output combining network and the inter-stage have been simulated using HP MOMENTUM. Due to the relatively important thickness of lines, the quasi-3D method has to be used to obtain accurate results [3], [4].

The stability of the circuit has been intensively studied using different methods. First, the conditions on Rollet factors of each individual stage has been verified (e.g. K>1 and B1>0 vs. process variations). Then the Nyquist Determinant Function (NDF) [5] analysis versus drain voltage has been performed and the different odd mode stabilizing elements (gate to gate and drain to drain) have been optimized. This insures safe operating conditions during drain bias pulse from 0 V to $V_D$max.

The circuit has been optimized between 5.0 GHz and 5.8 GHz to insure margins versus the 100 MHz application bandwidth.

The simulated linear performance of the circuit are presented in figures 2 and 3. The linear gain is greater than 28 dB and the return losses are better than –15 dB in the optimized frequency band (5-5.8 GHz).

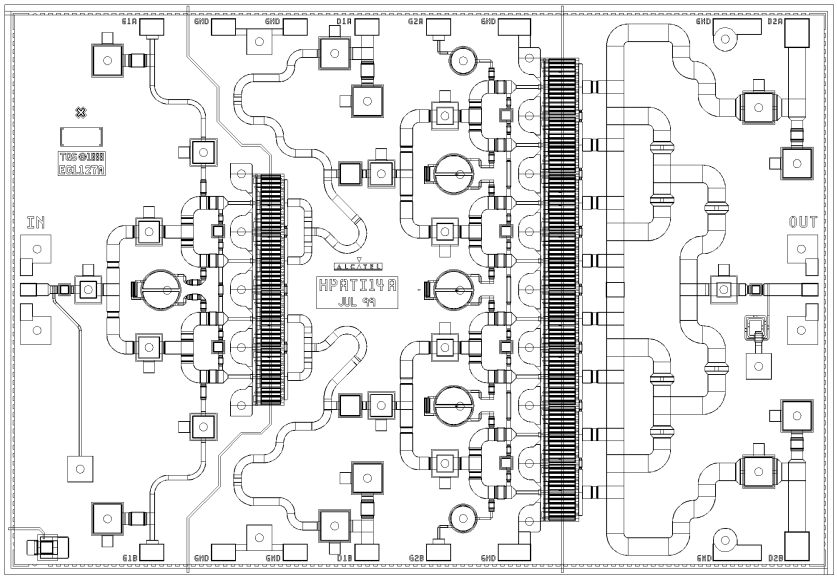

Fig. 1 : Layout of the chip (5.2x3.5 mm²)

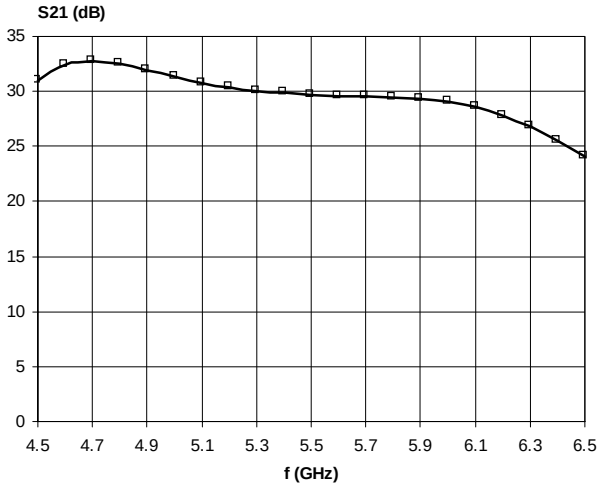

Fig. 2 : simulated S21 (dB) at V_D=8V

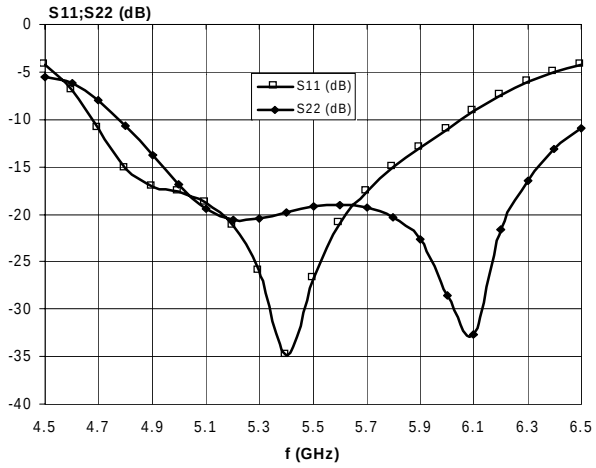

Fig. 3 : simulated S11 and S22 (dB) at V_D=8V

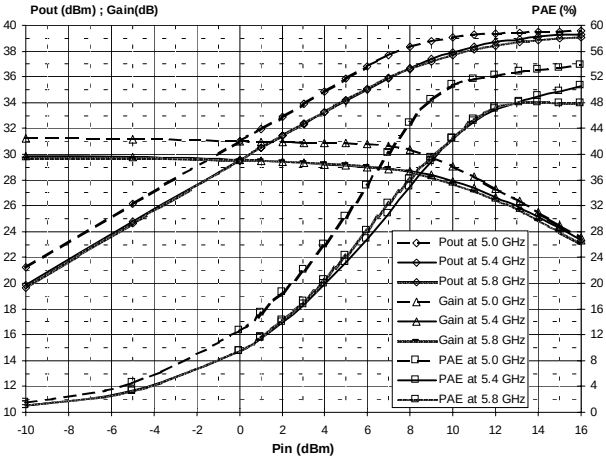

Fig. 4 : Simulated Gain, Output Power and PAE

The simulated non-linear performance of the amplifier are presented in figure 4. At 2.5 dB gain compression, the output power is greater than 38 dBm and the power added efficiency is better than 44 % over the 5.0 – 5.8 GHz frequency band.

III. MMIC MEASUREMENTS

Two types of measurements have been performed on this chip : On-wafer measurements and packaged MMIC measurements. RF probe measurements at Wafer level are realized on each MMIC under reduced bias conditions in order to avoid thermal problems. These measurements give a good assessment of the relative MMIC performance, but do not accurately

provide the values of the absolute performance. In order to accurately measure important parameters such as linear gain or output power, some representative dies of the whole lot, located at extreme and mean positions into the dispersion charts, have been fully characterized while mounted into a specific package providing thermal control and good RF interconnection accesses as shown on figure 5.

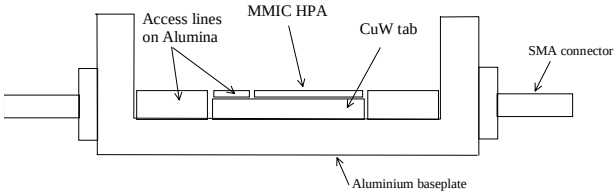

Fig. 5 : test fixture of the HPA

On Wafer measurement

RF probe measurements including linear and non linear characterization have been performed on every chip at Vd=6V.

Figures 6,7 and 8 exhibit the S-parameter measurements :

- Linear gain spread over production remains within 2dB between 5.0-5.8GHz
- Input reflection losses remains lower than –6.5dB within 5.0-5.8GHz
- Output reflection losses remains lower than –11dB within 5.0-5.8GHz

Figure 9 shows an output power spread over production of about 1.2dB at fixed input power.

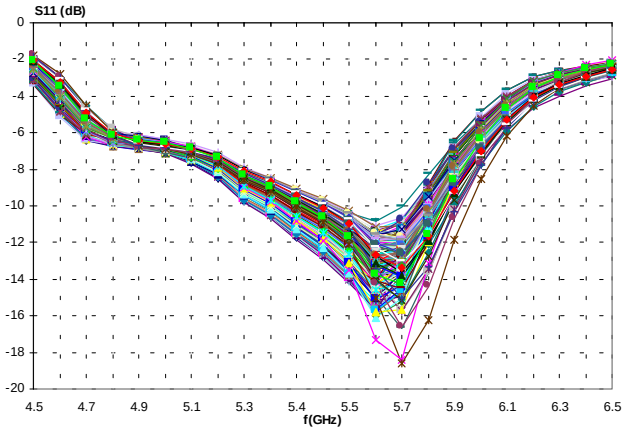

Fig. 6 : measured S11 (dB) at V_D=6V ambient temperature over production

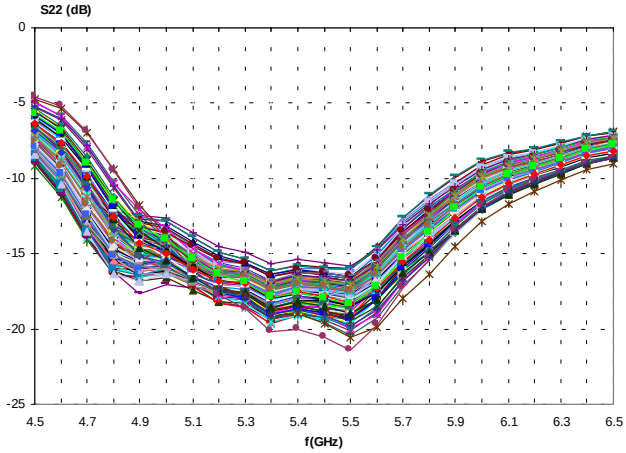

Fig. 7 : measured S22 (dB) at V_D=6V ambient temperature over production

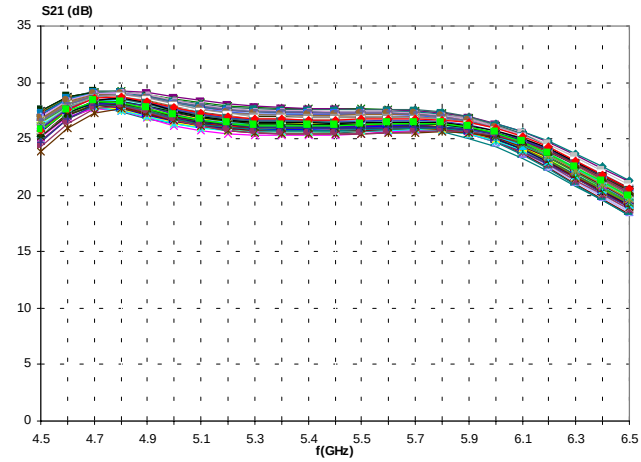

Fig. 8 : measured S21 (dB) at V_D=6V ambient temperature over production

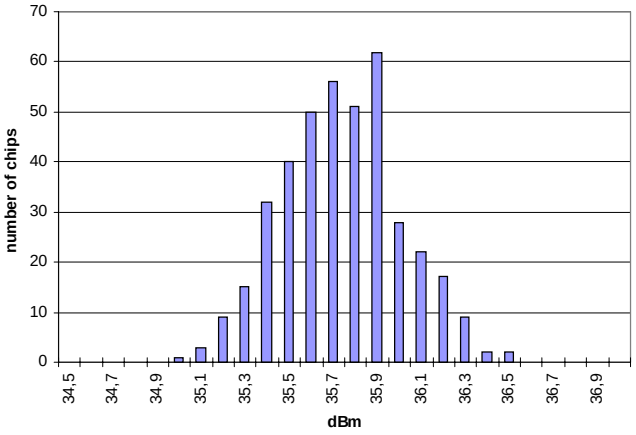

Fig. 9 : Output power spread at V_D=6V ambient temperature over production

Packaged MMIC measurement in pulsed mode

The measurements presented figure 10 and 11 have been performed on a die featuring average performances, i.e. delivering a mean output power over production. Drain voltage pulse duration is 40us for a duty cycle of about 10%.

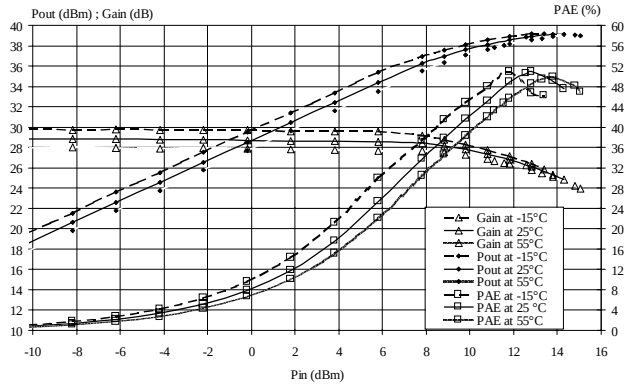

Fig. 10 : Pout, Gain and PAE versus Pin
3T (-15°C, 25°C, 55°C at bottom chip level)

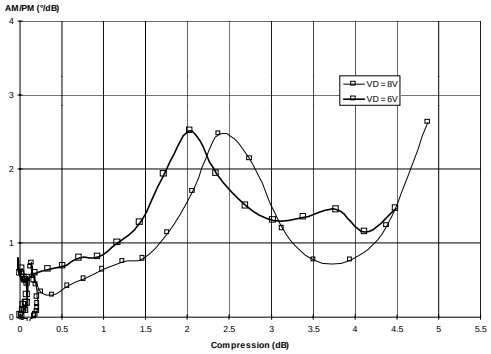

Fig. 11 : AM/PM versus compression state
T=-15°C (bottom chip level)

Output power, gain and PAE versus input power are shown on the figure 10 for 3 temperatures. Worst case output power is about 38.7dBm at 2.5dB compression with a PAE higher than 50%. Linear gain remains higher than 27.9dB at 55°C bottom chip temperature.

A very good agreement can be found between the non linear simulations and the pulsed measurements.

The figure 11 exhibits an AM/PM characteristic lower than 3°/dB at 5.4 GHz till 5dB compression in the worst case temperature conditions (-15°C at bottom chip level).

IV.CONCLUSION

The design and measurement of a high power MMIC C-band amplifier dedicated to space synthetic aperture radar applications has been presented. Power P-HEMT technology permits to achieve very high overall performance particularly on important criteria such as AM/PM conversion and power added efficiency. Due to their small size and high power density compared to hybrids, MMIC power amplifiers are a great prospect technology for satellite applications.

V. ACKNOWLEDGMENTS

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VI.REFERENCES

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