Monolithic Low-Noise Amplifiers up to 10 GHz in Silicon and SiGe Bipolar Technologies

student paper

Dietmar Zöschg[1,2], Wilhelm Wilhelm[1], Herbert Knapp[1], Klaus Aufinger[1], Josef Böck[1], T.F. Meister[1], Martin Wurzer[1], Hans-Dieter Wohlmuth[1], Arpad L. Scholtz[2]

[1]INFINEON Technologies AG, Otto-Hahn-Ring 6, D-81739 Munich, Germany,
Tel.: +49 89 234-48432, Fax.: +49 89 234-47069,
E-Mail: Dietmar.Zoeschg@infineon.com

[2]Institute of Communications and Radio-Frequency Engineering,
Technical University of Vienna, Gußhausstraße 25/389, A-1040 Vienna, Austria

Abstract— The noise properties of silicon and SiGe bipolar technologies at identical design rules are evaluated by theory and by experimental LNAs designed for the frequencies of 2 GHz, 6 GHz, and 10 GHz. For a fair comparison the same circuit principle is used for all six LNAs, with gain of about 20 dB or above, suitable for the applications in wireless communications.

I. INTRODUCTION

During the last years silicon-based bipolar technologies with highly improved RF performance have been developed. This is on one hand the new family of Si/SiGe bipolar technologies, on the other hand the well known silicon bipolar technologies have been scaled for lower parasitics and higher operating frequencies. In this work differences between silicon homojunction and Si/SiGe heterojunction devices for low-noise amplifiers are investigated by theory and by experimental LNAs. First the unique features of the used IC technologies are described, then the applied design principles are discussed. Finally the achieved experimental results are given and compared with the state of the art.

II. SILICON AND SIGE TECHNOLOGIES

The LNAs have been implemented in advanced silicon and SiGe bipolar technologies [1, 2], both with double-polysilicon self-aligned emitter base configuration and with effective emitter width of 0.25 μm. Both technologies use a lithography with 0.5 μm minimum feature size and 4 layer metallization scheme. The main difference between these two technologies is found in the formation of the active base: The base of the silicon transistors is formed by low-energy ion implantation with subsequent diffusion using rapid thermal processing. The resulting base width is only 50 nm with sheet resistance of 12 k$\Omega/\square$. Transit frequency of 52 GHz, maximum oscillation frequency of 65 GHz, and ECL gate delay of 12 ps are achieved. The base of the SiGe transistors is formed by selective epitaxial growth with maximum Ge content of 15 %. The Ge content is graded linearly across the base layer of 50 nm thickness. The intrinsic base sheet resistance is 4 k$\Omega/\square$, the transit frequency is 80 GHz, the maximum oscillation frequency is 97 GHz, and minimum gate delay of 8 ps (CML) is measured. Fig. 1 shows the schematic cross section of the transistors, the main transistor parameters for both technologies are summarized in Table 1.

III. CIRCUIT DESIGN

The circuit (see Fig. 2) consists of the input stage

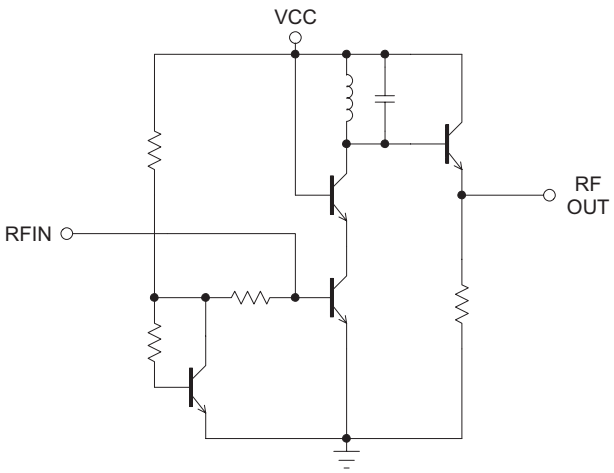

Fig. 2. Simplified circuit diagram for all LNAs.

in common-emitter configuration, the cascode stage for reduction of the Miller effect due to the base collector capacitance C_{BC}, the load realized as parallel resonance circuit, the output emitter follower stage, and the bias network enabling low supply voltages

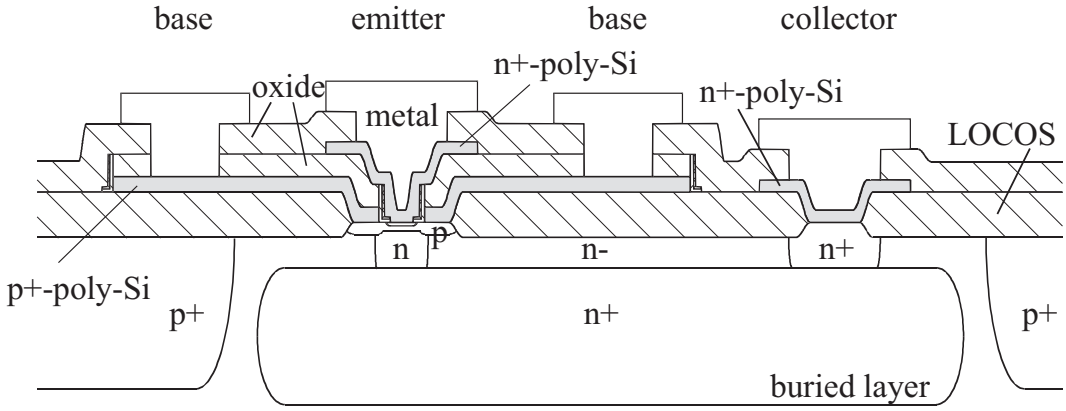

Fig. 1. Schematic cross section of the transistors.

Table 1. Main transistor parameters of the Si and SiGe technologies.

technology	Si	SiGe
min. lithographic feature size	0.5 μm	
max. cut-off frequency f_T	52 GHz	80 GHz
max. oscillation frequency f_{max}	65 GHz	97 GHz
min. gate delay τ_d	12 ps (ECL)	8 ps (CML)

down to 2.4 V. The noise figure is mainly determined by the input stage. In order to achieve the minimum noise enabled by the technology, the emitter length l_E of the input transistor has to be carefully scaled to get the optimum base resistance for the desired frequency band and for a 50 Ω source impedance. In this way the 50 Ω noise figure NF_{50} is close to the minimum noise figure NF_{min}. In addition, the collector bias current is set for minimizing the noise figure. The noise behavior is described on base of the transistor parameters and the model in Fig. 3 by

$$NF \approx 1+\frac{g_m \cdot Z}{2 \cdot \beta}+\left(1+\omega^2 C^2 Z^2\right)\cdot\left(\frac{R_b}{Z}+\frac{1}{2 \cdot g_m \cdot Z}\right). \quad (1)$$

β is the DC current gain, R_b is the base resistance, Z is the source impedance, g_m is the transconductance, and C is the input capacitance, formed by the parasitic transistor capacitance and the diffusion capacitance ($C = C_P + g_m \tau_F$). This reduces for low frequencies $f << f_T$ and $I_{C_{OPT}} = U_T\sqrt{\beta}/Z$ to

$$NF \approx 1+\frac{1}{\sqrt{\beta}}+\frac{R_b}{Z}. \quad (2)$$

Thus most important transistor parameters for the optimization of the circuits are the total base resistance R_b and the current gain β.

Expression 2 shows the potential of SiGe technologies which can have a lower base sheet resistance and a higher current gain β. However the term $1/\sqrt{\beta}$ is already rather small for advanced silicon technologies

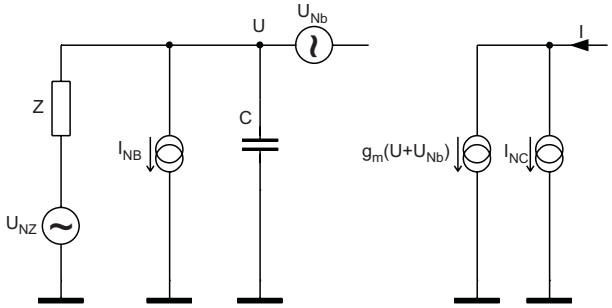

Fig. 3. Noise model for a single transistor stage.

($\beta \geq 100$). The total base resistance R_b, consisting of internal and external base resistance is for the here used small emitter widths dominated by the external base resistance which is about the same for both technologies. So the much lower base sheet resistance of the SiGe technology has minor importance for the total R_b[3].

For high frequencies the parasitic transistor capacitance ($C_P \approx C_{BE}$) is getting more important. The circuits were optimized under the assumption that $\tau_P = R_b \cdot C_P$ is constant for a fixed transistor geometry and for large emitter lengths ($l_E >> w_E$). This constant should be as small as possible. In order to minimize this constant τ_P of the parasitics, the configuration and layout of the input transistor is chosen to be base-emitter-base-collector (BEBC). The assumption that τ_P is constant and an optimisation leads to the conclusion, the optimal emitter

length decreases with increasing frequency for optimal noise matching.

With rising frequency the forward transit time τ_F takes more and more influence to the noise figure. The lower forward transit time τ_F ist the main advantage of SiGe technologies for low-noise amplifiers at high frequencies. This advantage is reinforced by the somewhat lower parasitic time constant τ_P of SiGe technologies.

IV. RESULTS

The noise figure NF_{50} and the gain have been measured on wafer for the 6 GHz and 10 GHz designs. The 2 GHz designs were measured on mounted chips. A photograph of the 2 GHz SiGe LNA is shown in Fig. 4. Fig. 5 gives the comparison of the

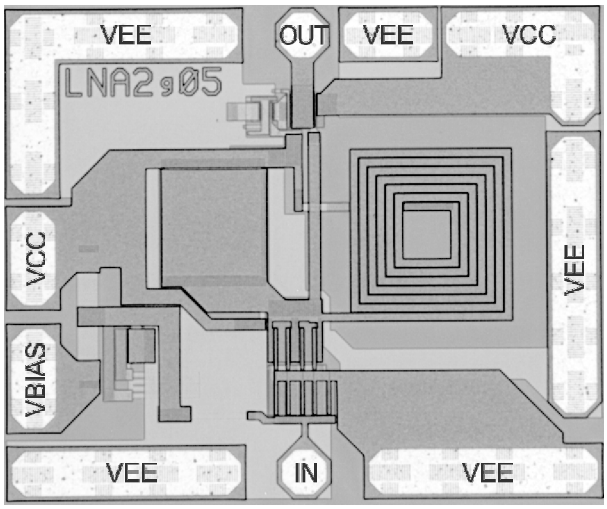

Fig. 4. Chip photograph of the 2 GHz LNA.

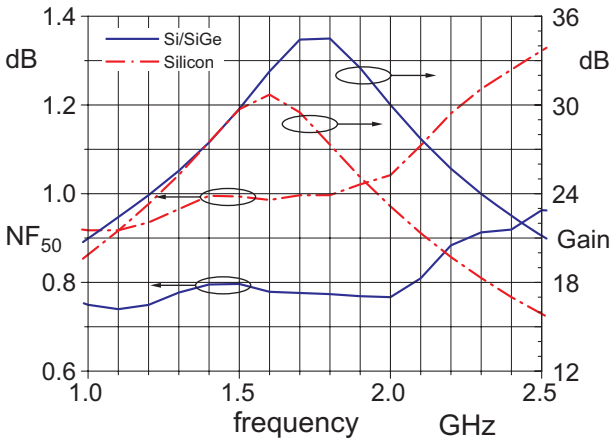

Fig. 5. Experimental results for the 2 GHz LNAs.

NF_{50} and gain values for the two 2 GHz designs. The SiGe circuit has advantages in gain (34.5 dB for SiGe vs. 30.7 dB for Si) and noise figure NF_{50} (0.8 dB for SiGe vs. 1.0 dB for Si). At 2 GHz there is a rather small difference for Si and SiGe designs. This is in agreement with the expectations mentioned before. The SiGe results are 1.3 dB at 6.2 GHz, and 2 dB at 10.5 GHz with high gains of 31 dB, and 26 dB, respectively. For silicon, noise figures of 1.8 dB for 5.6 GHz and 2.8 dB for 9.5 GHz with gain of 26 dB, and 21 dB are achieved. The measured results are summarized in Tab. 2. As can be expected from the designs with identical transistor configuration and size the power consumption for the two different technologies is nearly the same. At frequencies where the gain is getting small higher biasing for silicon technologies leads to larger power consumption.

Fig. 6 compares the state of the art [4–10] with the obtained results. Mainly due to the difference in the forward transit time the slope is different for the two technologies.

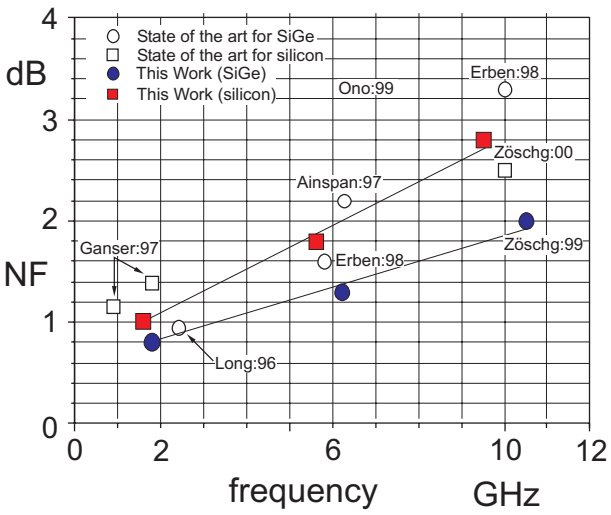

Fig. 6. Noise figure NF vs. frequency. Comparison of the presented noise results with the state of art for silicon-based bipolar technologies.

V. CONCLUSIONS

The noise properties of advanced silicon and SiGe bipolar technologies have been evaluated by monolithic LNAs for the frequencies of 2 GHz, 6 GHz, and 10 GHz. The circuits have been designed using a conventional circuit principle and precise input matching for the technologies.

The noise figures of 0.8 dB for 1.8 GHz, 1.3 dB for 6.2 GHz, and 2 dB for 10.5 GHz with high gains of 34 dB, 31 dB, and 26 dB, respectively, are setting a new state of art for SiGe technologies. For silicon the noise figures of 1 dB for 1.6 GHz, 1.8 dB for 5.6 GHz and 2.8 dB for 9.5 GHz with somewhat lower but still comfortable gains of 31 dB, 26 dB, and 21 dB are setting the new state of art. The results prove the increasing advantage of SiGe over Si with rising fre-

Table 2. Summary of the technical data of all LNAs.

Frequency band	2 GHz		6 GHz		10 GHz	
Technology (0.5μm)	Si	SiGe	Si	SiGe	Si	SiGe
Center frequency	1.6 GHz	1.75 GHz	5.6 GHz	6.2 GHz	9.5 GHz	10.5 GHz
50 Ω noise figure	1.0 dB	0.8 dB	1.8 dB	1.3 dB	2.8 dB	2.0 dB
Gain ($\|S_{21}\|^2$)	31 dB	34 dB	26 dB	31 dB	21 dB	26 dB
Power dissipation	22.8 mW	26.4 mW	31.3 mW	30.3 mW	36.5 mW	26.6 mW
Measurement	on mounted chips		on wafer			

quency. Due to the fact that silicon bipolar technologies are still in development a further reduction of noise figure is to be expected, and looking to the high gain achieved at 10 GHz, an extension to higher frequencies especially for LNAs in SiGe technologies is to be expected, too.

VI. REFERENCES

[1] J. Böck, H. Knapp, K. Aufinger, M. Wurzer, S. Boguth, R. Schreiter, T.F. Meister, M. Rest, M. Ohnemus, and L. Treitinger, "12 ps Implanted Base Silicon Bipolar Technology", *in IEDM Technical Digest*, pp. 553–556, December 1999.

[2] T.F. Meister, H. Schäfer, M. Franosch, M. Molzer, K. Aufinger, U. Scheler, C. Walz, M. Stolz, S. Boguth, and J. Böck, "SiGe Base Bipolar Technology with 74 GHz fmax and 11 ps Gate Delay", *in IEDM Technical Digest*, pp. 739–742, December 1995, TP 30.3.

[3] K. Aufinger, H. Knapp, R. Gabl, T. F. Meister, J. Böck, H. Schäfer, M. Pohl, and L. Treitinger, "Noise Characteristics of 0.5 μm/50 GHz Si and 0.5 μm/70 GHz SiGe Bipolar Technologies", *29th European Microwave Conference Proceedings*, vol. 2, pp. 129–132, October 1999.

[4] S. Ganser and S. Herzinger, "Silicon LNA/Mixer ICs for use up to 3 GHz", *Microwave Engineering Europe*, vol. 37, pp. 33–39, December/January 1997.

[5] Ono Masayoshi, Noriharu Suematsu, Shunji Kobo, Yoishitada Iyama, Tadashi Takagi, and Osami Ishida, "1.9 GHz/5.8 GHz-Band On-Chip Matching Si-MMIC Low Noise Amplifiers Fabricated on High Resistive Si Substrate", *IEEE MTT-S Int. Microwave Symposium Digest*, vol. 2, pp. 493–496, June 1999.

[6] D. Zöschg, W. Wilhelm, J. Böck, H. Knapp, M. Wurzer, K. Aufinger, H.-D. Wohlmuth, and A.L. Scholtz, "Monolithic LNAs Up to 10 GHz in Production-Near 65 GHz fmax Silicon Bipolar Technology", *in 2000 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers*, pp. 135–138, June 2000, MON4B-1.

[7] J.R. Long, M.A. Copeland, S.J. Kovacic, D.S. Malhi, and D.L. Harame, "RF Analog and Digital Circuits in SiGe Technology", *IEEE International Solid-State Circuits Conference*, vol. 39, pp. 52–54, February 1996.

[8] H. Ainspan, M. Soyuer, J.-O. Plouchart, and J. Burghartz, "A 6.25 GHz Low DC Power Low-Noise Amplifier in SiGe", *IEEE Custom Integrated Circuits Conference*, vol. , pp. 177–180, 1997.

[9] U. Erben, A. Schumacher, A. Schüppen, and J. Arndt, "Application of SiGe heterojunction bipolar transistor in 5.8 and 10 GHz low-noise amplifiers", *Electronics Letters*, vol. 34, pp. 1497–1500, July 1998.

[10] D. Zöschg, W. Wilhelm, T.F. Meister, H. Knapp, H.-D. Wohlmuth, K. Aufinger, M. Wurzer, J. Böck, H. Schäfer, and A.L. Scholtz, "2 dB noise figure, 10.5 GHz LNA using SiGe bipolar technology", *Electronics Letters*, vol. 35, pp. 2195–2196, December 1999.