A 70-GHz Bandwidth and 9-dB Gain Travelling Wave Amplifier Using 0.15-µm Gate InGaP/InGaAs HEMTs with Coplanar Transmission Line Technology

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***Abstract*- We developed a technique to reduce gain variations over a wide frequency range for an ultra-broadband travelling wave amplifier (TWA) that employs a cascode configuration using 0.15-µm gate InGaP/InGaAs HEMTs. Using this technique, we achieved gain variations within 1.5 dB for frequencies up to 70 GHz with a 9-dB gain. The agreement of measured S-parameters with simulated results demonstrates that the proposed technique is suitable for broadband amplifier design.**

I. INTRODUCTION

Recently, demand for commercially usable multimedia applications, such as Internet communication services and high-speed fiber optic communication subsystems that are capable of massive data transmission, has been rapidly increasing.

A travelling wave amplifier (TWA) is one of the key components in high-speed fiber optic communications, and TWA has potential for the subsystems. Several techniques to enhance the performance of TWA have been proposed, and they exhibited a capability for driving signal frequency from near the MHz to over 80 GHz [1]. However, the techniques have relatively large gain variations, especially at high frequencies. To achieve high-quality data transmissions, further improvements to TWA are necessary in order to reduce their gain variations over a wide frequency range as well as to achieve the broadband characteristics. The purpose of this paper is to present a technique that reduces gain variations with maintaining the circuit stability in TWA. Using this technique, we obtained gain variations of less than 1.5 dB for frequencies up to 70 GHz with a 9-dB gain from a TWA using 0.15-µm gate InGaP/InGaAs HEMTs. The output power was more than 13 dBm at 20 GHz and 40GHz.

II. CIRCUIT DESIGN

A. Gain flatness and circuit stability

To obtain broadband characteristics for TWA, we employed a cascode topology [1]. Figure 1 shows a schematic diagram of TWA. The circuit consists of two FETs. One is a common-source FET (CSF) and another is a common-gate FET (CGF).

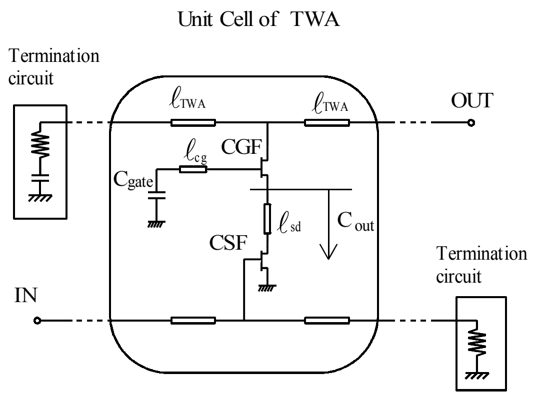

Figure 1. Schematic diagram of TWA.

According to Beyer et al. [2], the magnitude of the power gain in an amplifier stage can be described as follows:

$$G = \frac{g_m^2 R_{01} R_{02} \cdot \sinh^2[n(A_d - A_g)/2] \cdot e^{-n(A_d + A_g)}}{4[1+(\omega/\omega_g)^2][1-(\omega/\omega_c)^2]\sinh^2[(A_d - A_g)/2]} \qquad (1)$$

$$\omega_g = 1/R_i C_{gs}, \omega_c = 2/\sqrt{L_{TWA} C_{gs}}$$

$$L_{TWA} \approx \frac{Z_0 \cdot \ell_{TWA}}{\lambda_g \cdot f}$$

Here R_{01} and R_{02} are the image impedances of the input and output transmission lines, respectively, n is the number of unit cells in the amplifier, A_g and A_d are the attenuation factors on the input and output transmission lines, respectively.

In formula (1), $e^{-n(A_d+A_g)}$ is the dominant factor determining gain-flatness and circuit stability of the TWA. A_g and A_d are expressed as follow [3]:

$$A_g = \frac{(\omega_c/\omega_g)X_k^2}{\sqrt{1-[1-(\omega_c/\omega_g)^2]X_k^2}} \qquad (2)$$

$$A_d = \mathrm{Im}\left[1+\frac{j\omega L_{TWA}}{2Z_{out}}\right] \Bigg/ \sqrt{1-\mathrm{Re}\left[1+\frac{j\omega L_{TWA}}{2Z_{out}}\right]^2} \qquad (3)$$

Where, Z_{out} is the output impedance of a cascode HEMT [1].

$$Z_{out} = \frac{Z_{ds}+j\omega L_{sd}}{Z_{ds}+j\omega(L_{cg}+L_{sd})+1/j\omega C_{gs}+1/j\omega C_{gate}} \cdot \left(\frac{g_m Z_{ds}}{j\omega C_{gs}}+j\omega L_{cg}+\frac{1}{j\omega C_{gs}}+\frac{1}{j\omega C_{gate}}\right)+Z_{ds} \qquad (4)$$

$$L_{cg,sd} \approx \frac{Z_0 \cdot \ell_{cg,sd}}{\lambda_g \cdot f}$$

ω_g: gate-circuit radian cutoff frequency
ω_c: radian cutoff frequency of the line
C_{gs}: gate-to-source capacitance
R_i: effective gate-to-source resistance
ℓ_{TWA}: length of series transmission line for unit cell
Z_0: characteristic impedance of transmission line
f: frequency
λ_g: wavelength in the transmission line
$X_k=\omega/\omega_c$: normalized frequency
C_{gate}: capacitance connected at the gate of CGF
Z_{ds}: drain-to-source impedance of transistor
$L_{TWA,cg,sd}$: inductance of $\ell_{TWA,cg,sd}$

Frequency response of the A_g depends on parameters ℓ_{TWA} and C_{gs} of CSF. As for A_d, the dominant parameters are ℓ_{sd}, ℓ_{cg} and C_{gate}. In addition, these parameters also determine the stable conditions of TWA. When A_g+A_d is large negative, gain described in formula (1) would diverge, since the term $e^{-n(A_d+A_g)}$ diverges. As seen in formula (2), A_g is always positive at any frequency. Thus, determination of A_d profile is the key to improve the gain-flatness and stable operation over wide frequency range. Therefore, we focused on how to determine the parameters ℓ_{sd}, ℓ_{cg}, and C_{gate} of the TWA.

C_{gate} and ℓ_{cg} compose a resonant circuit. Since impedance looking into the CSF at source terminal of the CGF as shown in Figure 1, is always capacitive, C_{out}, the CGF including the resonant circuit composes positive feedback circuit. That means unstable circuit. This resonant frequency is determined by C_{gate} and ℓ_{cg} and C_{out}. To obtain a more stabilized condition, we set C_{gate} and ℓ_{cg} to small values in order to move the resonant frequency to higher region. Thereby, we can determine the gain flatness and circuit stability with ℓ_{sd}.

Figure 2 shows plots of A_g and A_d as a function of frequency with various ℓ_{sd} values. Here A_g doesn't change its profile by ℓ_{sd}, because the Miller capacitance of cascode HEMT is very small. On the other hand, the A_d depends on the ℓ_{sd} value. We paid attention to the frequency, f_x, where $A_d+A_g=0$. If the f_x is high, gain variations are small for a wide frequency range.

For a large ℓ_{sd}, A_d drastically increases at relative low frequency. Then the f_x is low. For small ℓ_{sd}, however, the A_d diverges into a large negative value, and the A_g+A_d is also negative. This will cause unstable operation. Consequently, large variations are yielded in the gain profile at high frequency. The optimum condition for ℓ_{sd} obtaining the gain-flatness and stable operation in the TWA is that A_g+A_d is small value over wide frequency range and a frequency f_x is set to higher region. We obtained the optimum value for the ℓ_{sd} as 60 μm in the case for our HEMTs.

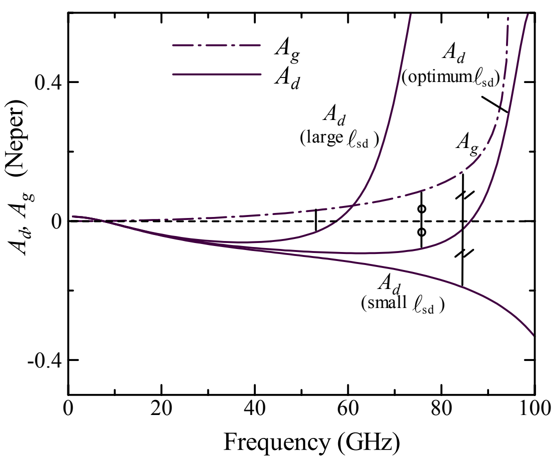

Figure 2. The calculated attenuation factor of input and output transmission lines (A_g, A_d).

B. Number of unit cells

When the number of unit cells of the TWA are increased, the gain-flatness deteriorate because of increasing an absolute value of $e^{-n(A_d+A_g)}$ in formula (1). If we maintain A_g+A_d as small as possible, we could reduce the affection by the number of unit cells. Therefore, we chose the minimum number of unit cells that could obtain the maximum GBWP value. Figure 3 shows simulated results of total gain and GBWP of the TWA as a function of the number of unit cells. The gain and GBWP are monotonically increased up to five cells, while the GBWP no longer increase beyond five cells. From the point of view improving the gain-flatness, it is preferable to choose five cells. Thus, we determine our TWA with five unit cells.

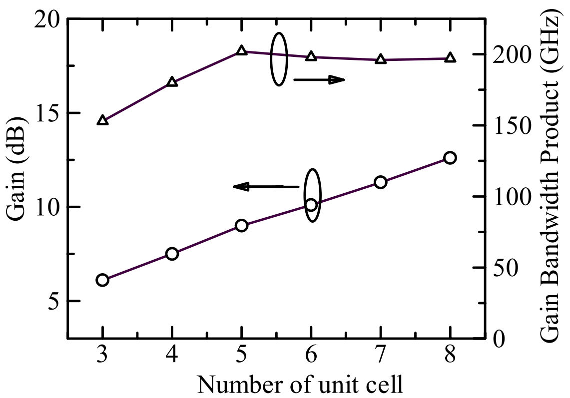

Figure 3. Number of unit cells.

III. FABRICATION

The 0.15-μm InGaP/InGaAs HEMT [4] in our TWA design provides a cutoff frequency of 95 GHz and a maximum oscillation frequency of 220 GHz for an 80 μm gate width. The HEMT was fabricated by electron-beam (EB) lithography, and T-shaped gate metal was formed on a semi-insulating GaAs substrate, as shown in Figure 4.

In the TWA design, we used coplanar waveguide (CPW) transmission line technology. Both the line width and gaps of CPW are 20 μm. The characteristic impedance, Z_0, is 52 ohm, the effective dielectric constant, Eeff, is 5.6, and losses are 0.17 dB/mm at the frequency of 50 GHz. Figure 5 is a microphotograph of the fabricated chip. The chip size is 1.0 mm x 2.0 mm.

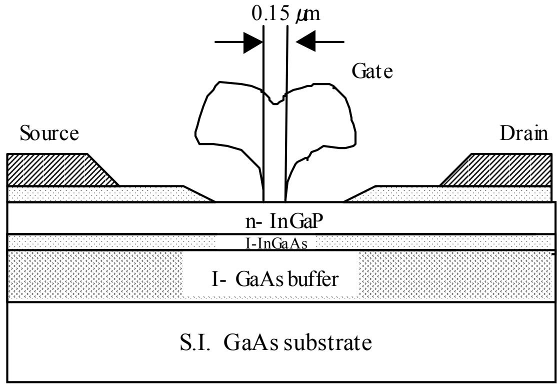

Figure 4. Cross sectional views of 0.15 μm gate InGaP/InGaAs HEMT.

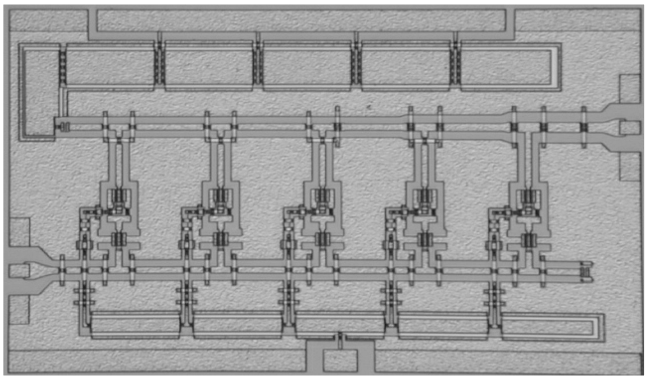

Figure 5. Microphotograph of the TWA with 5cells. The chip size is 1.0 mm x 2.0 mm.

IV. CIRCUIT PERFORMANCE

We measured S-parameters in a frequency range of 250 MHz to 110 GHz using a vector network analyzer HP-8510XF. RF-probes were calibrated using the LRRM maethod. Figure 7 shows the measured and simulated S-parameters. The resulting curves show a good agreement between theory and measurement. The amplifier has a gain of 9 dB with a 3-dB bandwidth of 70 GHz. A gain variation within 1.5 dB was achieved. Thus, the technique that we used is shown to be effective at reducing gain variations for frequencies up to 70 GHz.

We also measured Pin-Pout characteristics, as shown in Figure 7. The output power is about 13 dBm at frequencies of 20 GHz and 40 GHz. In addition, measured P_{1dB} was 9dBm.

Figure 8 illustrates the measured noise figure as a function of frequency. The noise figure has an average of 5 dB1 dB across a frequency band of 2 to 40 GHz.

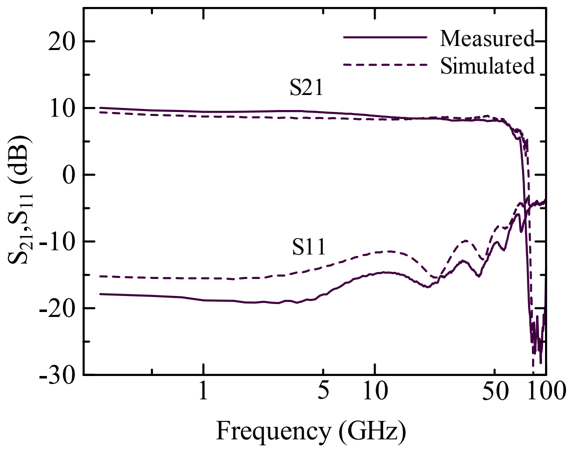

Figure 6. Measured and simulated S-parameters of TWA

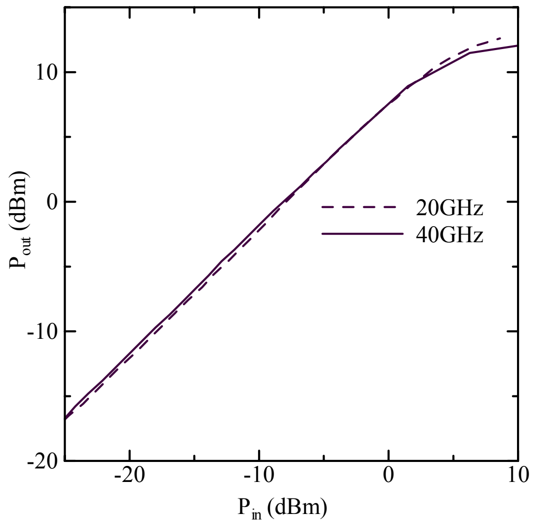

Figure 7. Measured output power versus input power at frequencies of 20 GHz and 40 GHz.

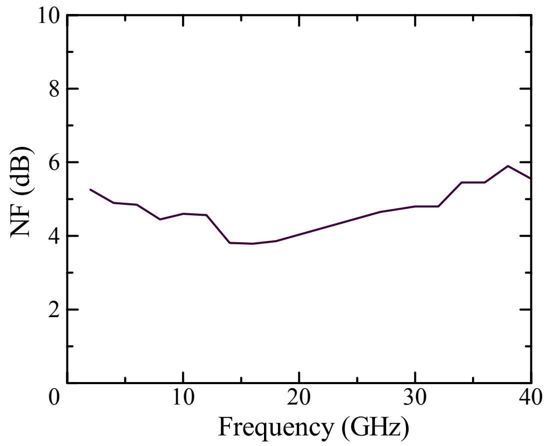

Figure 8. Measured noise figure of TWA.

V. CONCLUSIONS

We have designed and fabricated a TWA. To reduce gain variation as a function of frequency, we paid attention for A_d+A_g to have small variation over broadband frequency range. As a result, our TWA design has successfully reduced the gain variation within 1.5 dB for frequencies up to 70 GHz. Our amplifier is a likely candidate for use in high-speed fiber optic communication subsystems.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

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