

A J-band Transceiver MMIC with image rejection

C. A. Zelle, P. A. Gould*, P. D. Munday and R. W. Ashcroft

DERA, Malvern, Worcestershire, United Kingdom

*Bell Laboratories, Lucent Technologies, Swindon, UK.

Email: cazelle@dera.gov.uk

Abstract - This paper describes a J-band (15 GHz) transceiver MMIC with image rejection that has been designed for RADAR T/R module applications. The MMIC consists of a switched attenuator, an LNA, a Transmit/Receive switch, an image rejection mixer and a local oscillator buffer amplifier. The size of the MMIC is 6.48 mm by 4.47 mm. In receive mode the MMIC has a conversion gain in excess of 10 dB with less than 1 dB of ripple and noise figure less than 4 dB across a 10 GHz to 16.5 GHz band. The Input P1dB is -13 dBm. In transmit mode the conversion gain is -12 dB with an input P1dB of +15 dBm. The Transceiver MMIC was fabricated using the GMMT, 0.25 mm, H40 pHEMT process. This is believed to be the first integrated transceiver MMIC designed specifically for this frequency band.

I. INTRODUCTION

There is an increasing interest in J-band frequencies for both communication and radar applications. At J-band module spacing in phased array applications dictates an integrated RF solution. Monolithic Microwave Integrated Circuits (MMIC) are an important technology for realising cost effective circuit functions in a small area. They offer increased reliability and increased uniformity between modules. As the technology matures there is a trend towards increased levels of functionality on the MMICs. This increased functionality is accomplished through greater integration. In this paper a J-band transceiver MMIC, which has a high level of functionality realised through the integration of a number of circuit blocks, is presented. Many previous transceiver MMICs have focused on the lower communication bands below 5 GHz [1], [2] and [3]. At higher frequencies a multi-chip module approach has been used, [4], [5]. Integrated transceivers MMIC have been presented [6], [7] and [8], for X-band and K-band applications. The transceiver MMIC presented here is believed to be the first integrated transceiver designed specifically for use at J-band.

A description of the design and performance of the individual circuit blocks is given, followed by a

description of the integrated transceiver. The design approach is described and the transceiver performance is presented. The integrated transceiver MMIC circuit consists of a switched attenuator, an LNA, a Transmit/Receive switch, an image rejection mixer and a LO buffer amplifier. A chip photograph and functional block diagram is given in Fig. 1 and Fig.2 respectively. An image rejection mixer is used so that the beam forming can be performed digitally.

II. DESIGN AND MEASUREMENTS

The transceiver chip photograph and configuration are presented in Fig. 1 and Fig. 2. The integrated transceiver MMIC circuit consists of a switched attenuator. The output of the switched attenuator forms the input to an LNA. The LNA is connected to an image rejection mixer via a Transmit/Receive switch. An image rejection mixer is used so that the beam forming functions can be performed digitally. The mixer is driven by an LO buffer amplifier. During transmit mode the switched attenuator is in a high attenuation state and the LNA is switched off, to reduce loop gain. The gate and drain bias lines for the different amplification stages of the LNA and LO buffer were combined and the control lines for the attenuator and switch were combined. This was done to reduce the number of DC bond pads on the chip, due to the problems of feeding the DC connections to the chip within the tight size constraints of the T/R module.

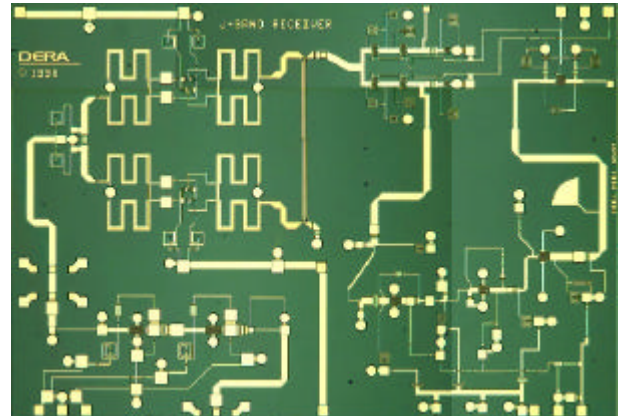


Figure 1, Photograph of the J-band transceiver MMIC

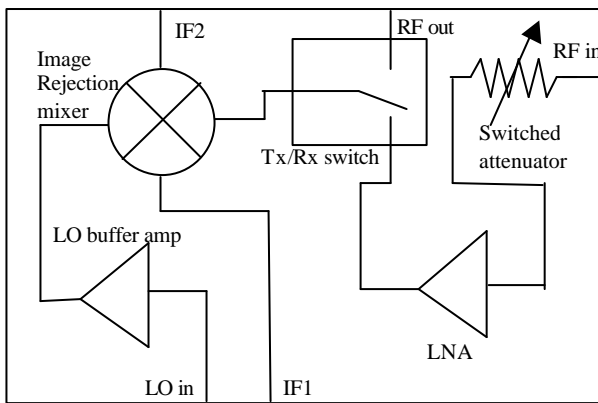


Figure 2, Block diagram of the J-band transceiver MMIC

The function of the switched attenuator is to protect the LNA amplifier and prevent feedback during Transmit mode. The attenuator contains three pHEMT devices arranged in a 'pi' configuration. Each transistor has an integrated spiral inductor connected across the source and drain terminals to resonate out the transistor parasitic capacitance. The shunt transistors are in series with 50 Ohm resistors, which ensure that a good match is maintained during the high attenuation state. The return losses for the attenuator between 10 GHz to 20 GHz is better than 10 dB in the 'on' state and better than 12 dB in the 'off' state. The 'off' state return loss between 13 GHz and 17 GHz was measured to be better than 20 dB. The switched attenuator has an isolation of greater than 20 dB from 13 GHz to 16.5 GHz and greater than 15 dB from 12 GHz to 18 GHz in the 'off' state. In the 'on' state an insertion loss of 1.0 dB was observed from 13 GHz to 18 GHz. The insertion loss at 12 GHz was 1.5 dB.

The Low Noise Amplifier has three stages and makes use of pHEMT transistors with a 0.25 μm gate length. The first two transistor stages use source degeneration to simultaneously provide low noise and a good input port match. The second and third stages make use of parallel LR feedback for gain shaping and stability. The Noise Figure of the LNA is less than 3 dB with a gain in excess of 22 dB from 10 GHz to 18 GHz. The LNA is biased using a single drain voltage of 3 V and a single gate voltage of -0.46 V. The bias current of the LNA circuit is approximately 160 mA. The LNA was matched to operate in a 50 Ohm environment. The input and output return loss was measured to be better than 15 dB from 12 GHz to 19 GHz.

The transmit/receive switch is a Single Pole Double Throw (SPDT) absorptive switch. It connects both transmit and receive paths of the transceiver to the mixer circuit. Each path contains two pHEMT transistors in series and a single shunt device. The shunt transistors are in series with 50 Ohm resistors so that a

good return loss is maintained at all the switch ports, regardless of switch settings. The drain-source parasitic capacitance of the devices are resonated out using spiral inductors. The each half of the switch circuit has an insertion loss of less than 2.5 dB from 12 GHz to 16 GHz. The insertion loss at 18 GHz is 2.7 dB. The return losses for the low attenuation part of the switch are better the 10 dB from 12 GHz to 20 GHz. The high attenuation path through the switch provides an isolation of 30 dB from 13 GHz to 15 GHz and an isolation of better than 26 dB between 12 GHz and 18 GHz. The return loss of the port connected to the common node via the high attenuation path is better than 17 dB from 12 GHz to 18 GHz.

The Image rejection mixer consists of two double-balanced mixers which are realised by configuring four 0.25 μm gate length pHEMT transistors as diodes by connecting the source and drain together. The diode rings are fed with balanced signals. The balanced signals are obtained using Marchand baluns realised using edge coupled, meandered transmission line. The design of these balun structures is believed to be original. The two double-balanced mixers are used as in-phase and quadrature channels. A 90 degree 3 dB signal split is produced through the use of a Lange coupler at the RF portion of the mixer. The LO signal is fed to the two mixers using an in-phase lumped Wilkinson divider. The mixer has an in-phase and quadrature IF output which are combined using an off-chip IF quadrature coupler. The Image rejection mixer has a conversion loss of 8 dB and image rejection of better than 20 dB from 12 GHz to 18 GHz. The LO drive level required by the mixer is 15 dBm. The mixer ports are matched to 50 Ohms.

The LO buffer amplifier consists of two stages. Each stage contains a 0.25 μm gate length pHEMT transistor with parallel LR feedback. The amplifier has a gain of greater than 12 dB from 12 GHz to 18 GHz. The LO buffer amplifier is biased using a single drain supply voltage of 3.0 V and a single gate voltage of -0.3 V. The current consumption of the circuit is 240 mA. The amplifier was matched to 50 Ohms. The input return loss was measured to be better than 15 dB from 6 GHz to 17 GHz. At 18 GHz the input return loss was better than 10 dB. The output return loss was seen to be better than 15 dB from 12 GHz to 20 GHz.

The circuits blocks described above were designed using HP Eesof, for electrical simulation, Sonnet, for electromagnetic simulations and were laid out using Barnard microsystems Wavemaker. Great care was taken during lay out to minimise electromagnetic coupling between adjacent components. Each circuit was simulated extensively to assess performance against temperature and process variations, prior to integration. Then extensive simulations were performed on the

integrated circuit. A chip photograph of the integrated circuit is presented in Fig. 1.

III. INTEGRATED MMIC MEASUREMENTS

The integrated transceiver MMIC size is 6.48 mm x 4.47 mm. The MMIC is biased using a drain voltage of 3 V, with a total required current of 400 mA. The LO input port return loss was measured to be better than 10 dB from 10 GHz to 17.5 GHz, as seen in Fig 3. The performance of the transceiver can be separated into two modes, receive mode and transmit mode.

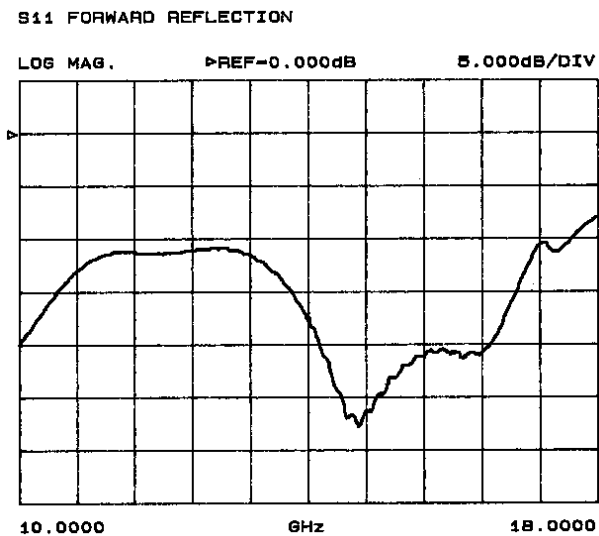


Figure 3, LO input port return loss

A. Receive mode

The overall Noise Figure of the MMIC was less than 4 dB with an associated conversion gain greater than 10 dB with less than 1 dB ripple (see Fig. 4). The LO drive level required by the chip is +4 dBm. The level of image rejection achieved is better than 20 dB (using an external quadrature coupler). The LO to IF isolation was measured to be 48.17 dB and the RX to IF isolation was measured to be 32.0 dB, at 15 GHz. The Input 1 dB compression point was measured to be -13 dBm.

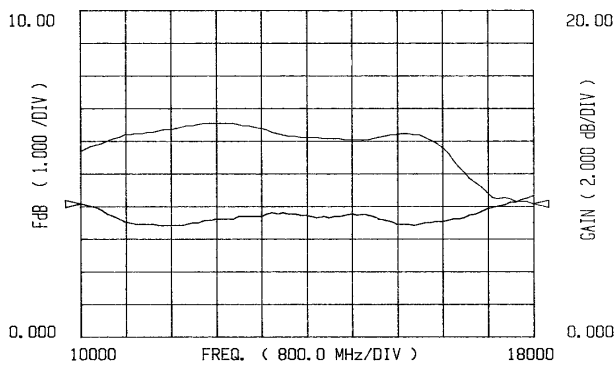


Figure 4, Noise figure and Gain in receive mode

In receive mode the return losses of the transmit and receive ports were measured to be better than 7 dB across the band, as seen in Fig. 5 and Fig. 6. The Rx port match was worse than expected at approximately 15 GHz. This is believed to be due to the chip numbering text that was placed close to the LNA input line prior to mask fabrication. The port match measurements of the individual LNA block gave excellent agreement with simulations.

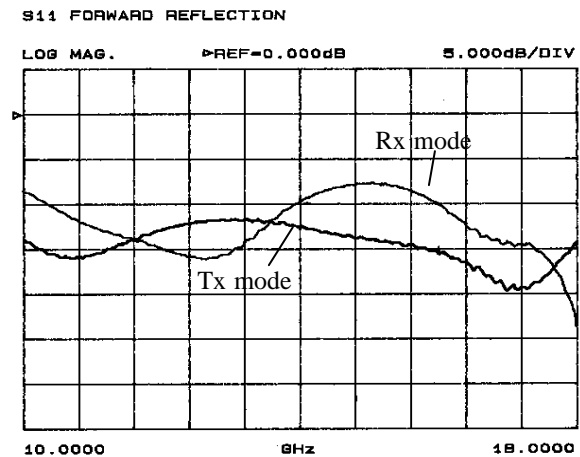


Figure 5, Receive port return loss

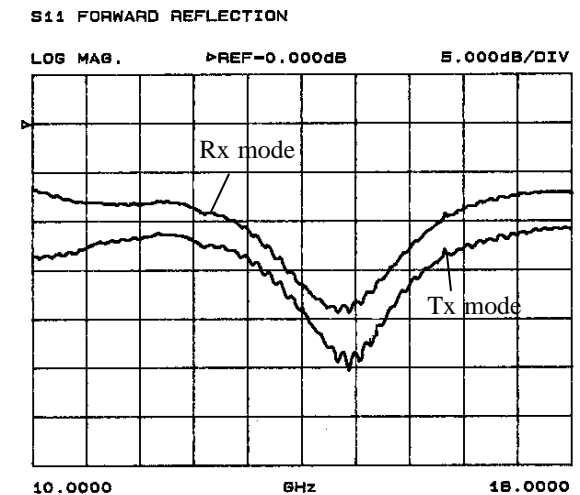


Figure 6, Transmit port return loss

B. Transmit mode

The insertion loss of the transceiver in transmitter mode is -12 dB. The image rejection achieved is better than 20 dB (using an external coupler). The LO to TX isolation was seen to be 36.67 dB, at 15 GHz. The Rx to Tx isolation at 15 GHz was 41.45 dB with the LNA switched off. In transmit mode the input 1 dB compression point was measured to be +15 dBm. In

transmit mode the return loss of the transmit and receive ports was better than 10 dB across the band, as seen in Fig. 5 and Fig. 6.

IV. CONCLUSION

In this paper a J-band transceiver MMIC with image rejection has been described. The MMIC consists of a switched attenuator, a low noise amplifier (LNA), a Transmit/Receive switch, an image rejection mixer and a local oscillator buffer amplifier. The size of the MMIC is 6.48 mm by 4.47 mm. In receive mode the MMIC has a conversion gain in excess of 10 dB and an associated noise figure less than 4 dB across a 10 GHz to 17 GHz band. The level of image rejection achieved was seen to be better than 20 dB. The Transceiver MMIC was fabricated using the GMMT, 0.25 μm gate length, H40 pHEMT process. The circuit contained a high level of integration, which was demonstrated to give excellent performance. The MMIC described is suitable for RADAR T/R module applications in the 10 GHz to 17 GHz band. This is believed to be the first integrated transceiver MMIC designed specifically for this frequency band.

V. ACKNOWLEDGEMENTS

The authors gratefully acknowledge the contributions of Mark Moore, Geoff Ball, Andy Wicks and Greg Ball.

VI. REFERENCES

- [1] T. Quach, F. Bonn, J. Ortiz, M. Thomas, "A highly integrated commercial GaAs transceiver MMIC for 2.45 GHz ISM applications", pp 141 IEEE WCC, 1997.
- [2] J. Komiak, A. Agrawal, "Octave S/C band MMIC T/R modules for multifunction phased arrays", pp. 35, IEEE MMWMC-S, 1991.
- [3] H. Ma, *et al.*, "A single chip 1.9 GHz RF transceiver MMIC using GaAs MESFET technology", pp. 101, IEEE RFIC-S, 1998.
- [4] M. Kanno, et al., "Miniturised X-band MMIC T/R module for conformal array antenna", pp. 17, IEEE MTT-S, 1996.
- [5] J. Bugeau, W. Coughlin, M. Priolo, G. Onge", Advanced MMIC T/R module for 6 to 18 GHz multifunction arrays pp. 119, IEEE MMWMC-S, 1992.
- [6] I. Toyoda *et al.*, "X-band Si Bipolar transistor single chip transceiver using three-dimensional MMIC technology" pp. 337, IEEE MTT-S, 1998.
- [7] T. Sakia, N. Takeuchi, A. Mizobuchi, Y. Iyama, N. Tanino, "Ultra small size X band MMIC T/R module for active phased array", pp. 1531, IEEE MTT-S, 1992.
- [8] H. Fudem, S. Moghe, G. Dietz, S. Consolazio, "A highly integrated MMIC K-band transmit/receive chip", pp. 119, IEEE MMWMC-S, 1993.