

10W C-BAND HIGHLY EFFICIENT HYBRID-MMIC AMPLIFIER

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ABSTRACT - A very high efficient, low distortion C-band Hybrid-MMIC Amplifier using linear and non-linear models of the PHEMT devices has been developed. Double stage Hybrid-MMIC amplifier fabricated with 2x3.6mm gate width PHEMT and 2x12mm gate width PHEMT exhibits a power output of 40.2 dBm at 2dB of gain compression, a linear gain of 26dB and an associated PAE of greater than 46% in the frequency range of 3.8-4.2GHz.

These excellent results are obtained by developing an accurate non-linear model of the PHEMT device and optimizing the output-matching network of the amplifier by using a high dielectric substrate with low insertion loss.

I. INTRODUCTION

In digital modulation communication systems, the highly time-varying envelope of the RF input signal has to be amplified with low loss distortion to fulfill the requirement on the bit-error rate. Therefore, the power stage of the transmitter amplifier of satellite equipment requires not only high power added efficiency for optimum dc-power handling, but also high linearity, both requirements are contradictory. In order to increase linearity, a conventional amplifier usually has to be driven with a sufficient input power back-off, whereas high PAE can only be achieved when the amplifier operates in gain compression [1].

PHEMT devices are becoming a very attractive choice for use in microwave power amplifiers due to specific characteristics such as high gain, linearity and high output power [2] [3] [4] .

In recent years, power amplifiers have been designed using full MMIC approach to achieve low cost and wide band operation [5] .

The design of Hybrid-MMIC amplifier has the following advantages over the full MMIC approach:

- Fewer losses for the output matching network (0.5dB improvement)
- Improved harmonics load
- Fine tuning of the output stage to compensate for manufacturing dispersion.

In this paper, we present the results of a Hybrid-MMIC amplifier at C-band using PHEMT devices to achieve a power output of 10W, a linear gain of 26dB with an associated Power Added Efficiency (PAE) of greater than 46%.

I . AMPLIFIER DESIGN

Electrical simulations:

The small and large signal device models are used in the design of the power amplifier.

A small cell of 1.5mm periphery is characterized with small-signal S parameters measurements and DC pulse tests. These measurements allow extracting the electrical parameters of linear and non-linear models. General rules of scaling are used in order to obtain the electrical model parameters of power PHEMT devices used in the power MMIC [6] .

Figure1 shows the simplified schematic of the two-stage amplifier. The first stage employs two times 2 cells of 12-finger, 1800 μ m PHEMTs and the second stage has two times 8 cells of 12-finger, 1500 μ m PHEMT devices (0.25 μ m PHEMT from Triquint Semiconductor Texas). To reduce the chip size, the input and the intermediate matching networks are

designed in MMIC by using shunt capacitors with integrated vias.

To avoid imbalance operation, each couple of PHEMT is connected by gate and drain stabilizing resistors. To obtain the optimum power performance, a load pull simulation was performed with in-house model using Libra simulator. The output stage is designed on a high dielectric substrate with low insertion loss, in order to reduce the output section losses and optimize the matching network by a small additional tuning.

From calculated optimum load reflection coefficient and S-parameters at the device level (for achieving the maximum PAE), we determined the source and the load equivalent circuits. Then the matching networks of the power amplifier are optimized by the harmonic balance simulator (Libra of HP-Eesof) to achieve the optimum combination of high output power and high PAE [7] [8].

A full wave electromagnetic simulation (Momentum) was performed for passive structures to eliminate the uncertainties caused by the quasi-static models.

The RF and DC decoupling as well as the bias circuits are included in the Hybrid-MMIC amplifier to make it a self-content module without the need of outside circuitry. The layout of the amplifier is shown in the figure 2.

The simulated AM/AM response of the power MMIC (under $V_{ds} = 7V$, $I_{ds0} \approx 2A$) is shown in the figure 3. The output power is higher than 40 dBm, with the associated PAE greater than 50% over the frequency range of 3.5-4.4GHz. The unconditional stability of the power module was checked by using the K-factor and the NDF methods [9] [10].

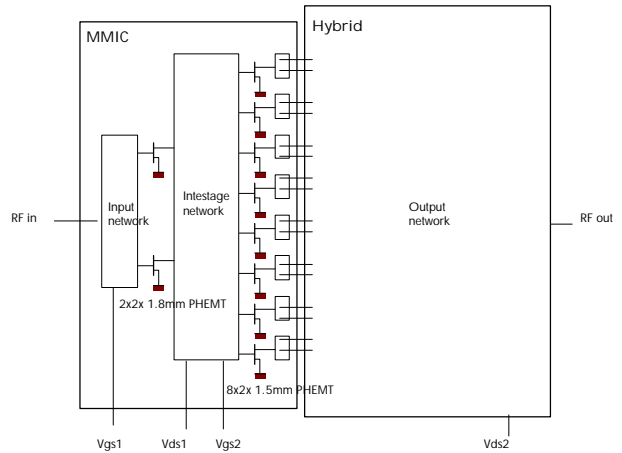


Figure 1: simplified schematic of the power amplifier

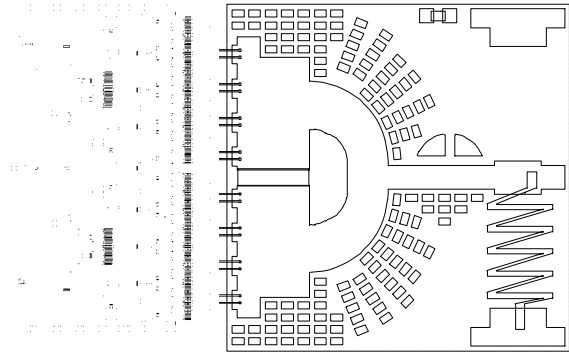


Figure 2: Layout of the power amplifier

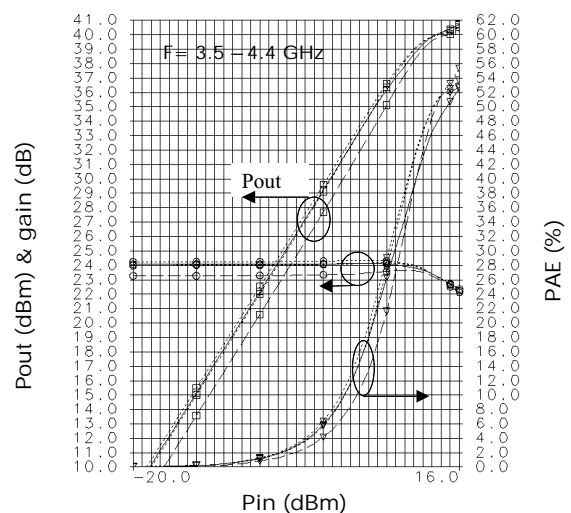


Figure 3: Simulated P_o , gain and PAE (under $V_{ds} = 7V$, $I_{ds0} \approx 2A$).

Mastering the non-linear model allows simulating the instantaneous non-linear gate forward current and gate-drain breakdown voltage to check that the power module is designed in a safe operating area. Because reliability is of extremely high importance for space application, this methodology is a major advantage over the more classical approach based on life test data only.

The maximum drain-gate voltage swing (simulation at $V_{ds}=7V$) at 2dB gain compression is less than 15.5V, far much less than the specified maximum derating voltage.

This analysis demonstrates that the power module can operate at 2dB of gain compression without any impact on the reliability of the device.

Thermal simulations:

Two thermal models have been realized using the IDEAS simulator. The first model is designed by taking into account the topology of the power MMIC, the thickness of the layers, etc. The second model is designed for the hybrid module by brazing the MMIC chip, the MIC substrate and the decoupling capacitors on the Bottom of the package as is shown in the figure 4.

Taking into account the thermal resistance's of the chip devices obtained from the first model, of the Cu/W carrier, etc, the dissipated power for the hottest spot temperature of 115°C is 14W as is shown in the figure 5 (the reference temperature is 65°C).

I . EXPERIMENTAL RESULTS

The measured linear performance of the packaged Hybrid-MMIC amplifier under CW signal excitation is shown in figure 6. The linear gain is greater than 25dB over the frequency range of 3.7-5GHz.

The corresponding power performance is shown in the figure 7.

The power output is 40.2dBm at 2dB of gain compression with a linear gain of 25dB and the associated PAE greater than 46% over the frequency range of 3.8-4.2GHz (biasing condition: $V_{ds}=7V$). These measurements do not take into

account the losses of the test jig (insertion loss of the test jig $\approx 0.2dB$).

When the power amplifier is biased at $V_{ds}=8V$ as is shown in the figure 8, the power output increases to 41dBm(12.6W) at 2dB of gain compression with the associated PAE greater than 43% over the 3.8-4.2GHz frequency band.

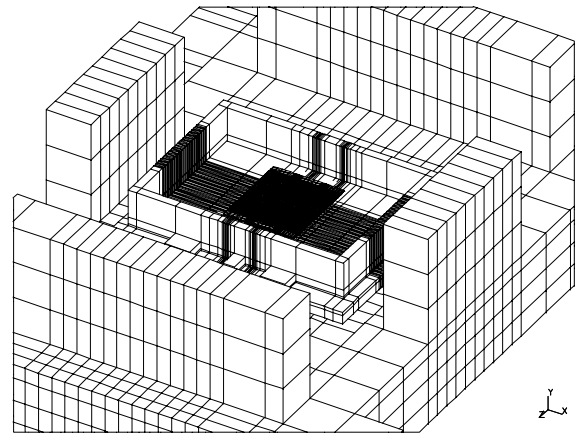


Figure4: Thermal model of the packaged amplifier

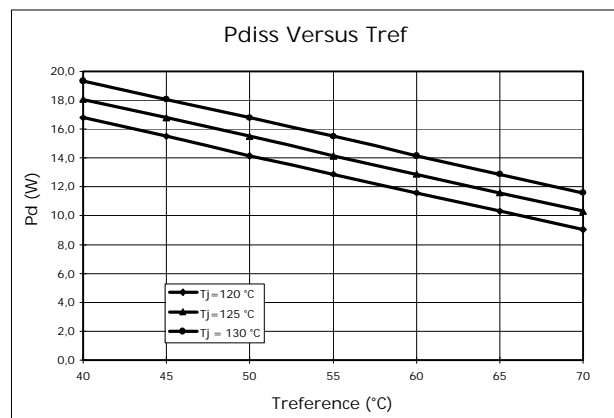


Figure5: Dissipated power as a function of Tref

IV. CONCLUSION

The use of power PHEMT devices and Hybrid-MMIC technology allows to achieve the best output power and PAE with good linearity and to minimize the weight and the size of the SSPA.

Using the comprehensive methodology developed by Alcatel, linear and non-linear electrical models of PHEMT chip devices were established. This work has allowed us to design a power Hybrid-MMIC module at C-band for space application.

V. ACKNOWLEDGMENTS

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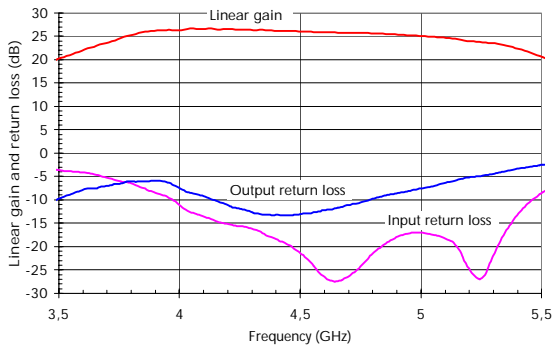


Figure6: Measured linear response of the 10W amplifier

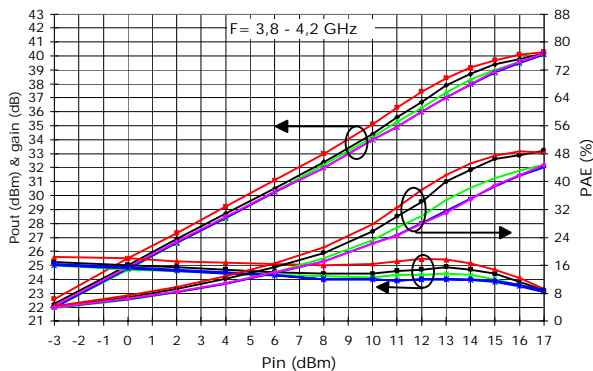


Figure 7: Measured Power Output, Gain and PAE versus Power Input of 10W Amplifier under CW signal excitation ($V_{d_s}=7V$).

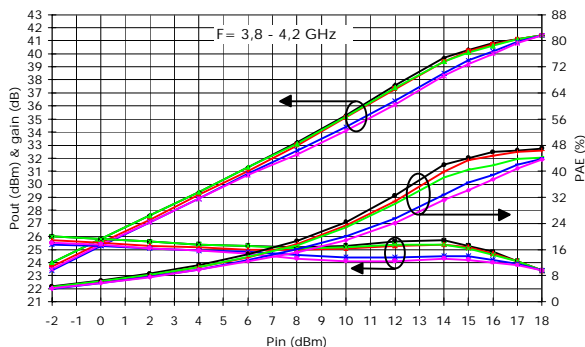


Figure 8: Measured Power Output, Gain and PAE versus Power Input of 10W Amplifier under CW signal excitation ($V_{d_s}=8V$)