A novel high Q active inductor for millimeter wave applications

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***Abstract* - The paper introduces an active inductor implementation suitable for microwave and millimeter wave applications. The proposed circuit exhibits a quality factor in excess to 500 at 25 GHz with a current consumption of 1.2 mA @ 1.5V bias. A Monolithic implementation in PHEMT technology is reported and discussed.**

I. INTRODUCTION

The implementation of high Q lumped inductors is highly desirable, particularly at microwave and millimeter-wave frequencies where the conductor losses dramatically increase with the operating frequency. Moreover, lumped-element spiral inductors usually exhibit a resonant behaviour, due to capacitive parasitics, well below millimeter wave frequencies. Such detrimental effects actually limit the potential improvements that a low-loss inductor may introduce in microwave circuits design. Potential applications include inductive peaking techniques to increase amplifier's operating bandwidth, filtering structures and many others.

A solution to this problem is in the synthesis of active inductors [1, 2, 3, 4], featured by reduced size and high quality factors. Many attempts have been proposed in the past, using a single active device or a combination of active devices, both in grounded and floating configurations [5,6,7,8].

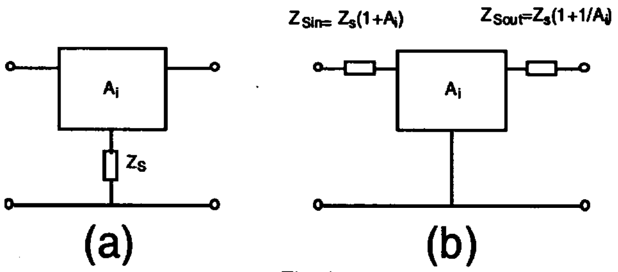


Fig. 1
Miller theorem equivalent circuit.

In this contribution a novel approach, based on the application of the Miller theorem, and allowing a major improvement in the inductor quality factor, Q, is presented. The proposed active inductor is well suited even for Ka-band applications and makes use of only few active elements. With a careful scaling of the selected active devices and with a suitable bias topology, the Q of the active inductor can be simply controlled varying the bias voltage.

II. BASIC THEORY

The well known Miller's theorem states that when a series impedance, Z_s, is connected between the common terminal of an amplifier with a current gain, A_i, and the voltage reference terminal (generally the circuit ground), the circuit is equivalent to the same amplifier with two impedances, Z_{sin} and Z_{sout}, in series to its input and output terminals as shown in Fig. 1, where:

$$Z_{sin} = Z_s \cdot (1 + A_i)$$

$$Z_{sout} = \frac{Z_s}{1+\frac{1}{A_i}}$$

If a Common-Gate FET is assumed as the core amplifier, its current gain, taking into account the gate to source capacitance of its equivalent-circuit representation, C,, can be approximately expressed by:

$$A_i = \frac{g_m}{g_m + j\omega C_{gs}}.$$

Let us assume that Z_s is an inductor with a series resistance representing its losses (Fig. 2):

$$Z_S = R + j\omega L.$$

Evaluating the Z_{sin} with the drain terminal shorted to ground, its real part can be reduced by increasing the FET transconductance, g_m, while its imaginary part is essentially the reactance of the initial inductor.

This high-Q inductor is actually in series to the gate-source capacitance that can be increased by a shunt-connected capacitor, and hence exploiting the inductive behaviour beyond the resonant frequency:

$$\omega_{RES} = \frac{1}{\sqrt{LC_T}} ,$$

where C_T is the total capacitance between gate and source terminals.

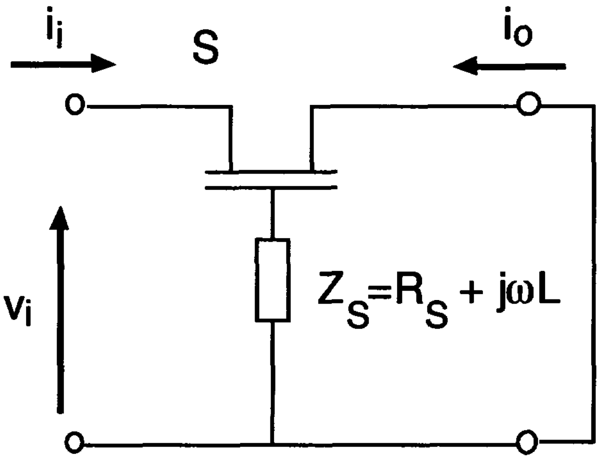


Fig. 2
The Common-Gate circuit with Z_s

Since a negative resistance is actually used to reduce the losses in the active inductor, the transistor g_m and therefore the device size must be carefully selected, in order to achieve the desired reduction of the losses and, at the same time, to avoid any possible instability.

For applications at millimeter-wave frequencies the passive inductor can be simply implemented using a narrow transmission line shorted to ground through a via hole, due to the low inductance values usually required in this frequency range.

III. DESIGN PROCEDURE

Once the desired value of inductance, L, is selected, a capacitance must be added in parallel to the gate source capacitance, C,, that usually results to be too small to guarantee a suitably low operating frequency for the active inductor. The total capacitance, in fact, must be selected to operate the circuit beyond the resonant frequency of the resulting LC series connection.

Depending on the values of L ,C_T, the losses R and the operating frequency, F, the value of the transistor transconductance, g,, must be selected in order to maximise the inductor's quality factor, Q:

$$Q = \frac{R \cdot g_m + \omega^2 \cdot L \cdot C_T}{\omega (R \cdot C_T - L \cdot g_m)} .$$

The function above grows for g_m ranging from 0 to the resonant value given by:

$$g_m = \frac{R \cdot C_T}{L}$$

This value of g_m represents the upper limit of stability for which the losses are equal to the modulus of the negative resistance produced by Ql. Thus, in order to maximise the active inductor Q, this condition has to be carefully approached avoiding a neat negative resistance and thus providing a suitable safety margin for circuit stability.

It is worth to note that the critical transconductance value is determined by losses, R, the inductance, L, and the capacitance C_T and can be fairly low, thus allowing for a corresponding extremely low bias current.

The active inductor performance are affected by the bias circuit. In our case the topology sketched in Fig. 3 has been adopted.

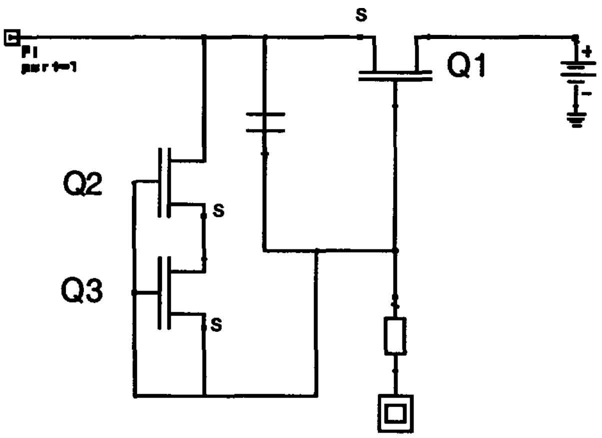


Fig. 3
The active inductor schematic.

The Common-Gate FET, Ql, has the gate terminal shorted to ground by a narrow transmission line and a via hole and the source biased by a couple of FETs, Q2 and Q3, being the drain directly connected to the power supply. As stated before, the connection in the gate circuit of Ql furnishes the inductance, L. The equivalent model of the biased active inductor is reported in Fig. 4, where the shunt resistor takes into account the loading of the two biasing transistors, Q2 and Q3, while the series R-L-C circuit models the active inductor according to what previously discussed. The shunt resistor, R_p, can be easily dimensioned to achieve values of the order of tens of KΩ, and minimising therefore the influence of the bias circuit over the inductor quality factor, Q.

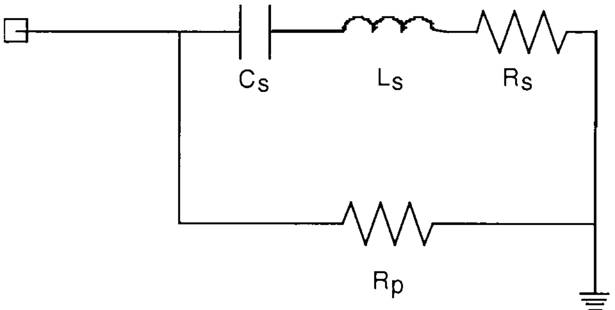


Fig. 4
Active inductor equivalent circuit.

IV. EXPERIMENTS

A prototype inductor has been designed using the Philips ED02AH PHEMT process. As sketched in Fig. 3, the inductor has been implemented with a short transmission line with its end shorted to ground through a via hole. The capacitor inserted in parallel to the gate-source capacitance is a MIM capacitor.

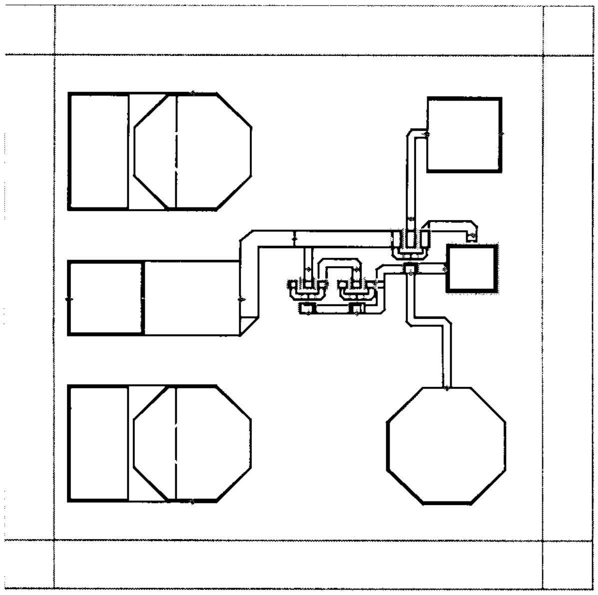


Fig. 5
MMIC layout: dimension 600 x 600 $\mu\ m^2$.

The PHEMTs have been modelled using a small-signal equivalent-circuit scalable model to carry out the dimensioning of the active inductor. A large signal SPICE model has been used to evaluate the inductor linearity and distortion.

The layout of the resulting active inductor is depicted in Fig. 5. The overall chip dimensions are 600 x 600 $\mu\ m^2$. It is worth to note that most of the die area is occupied by the coplanar pads ensuring very compact dimensions for the active inductor.

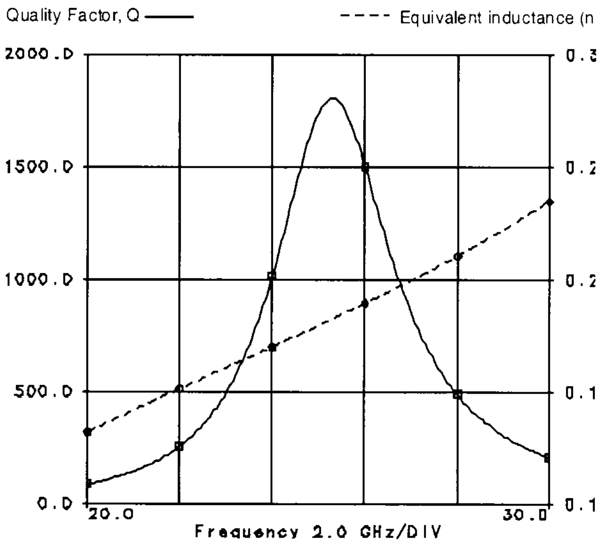
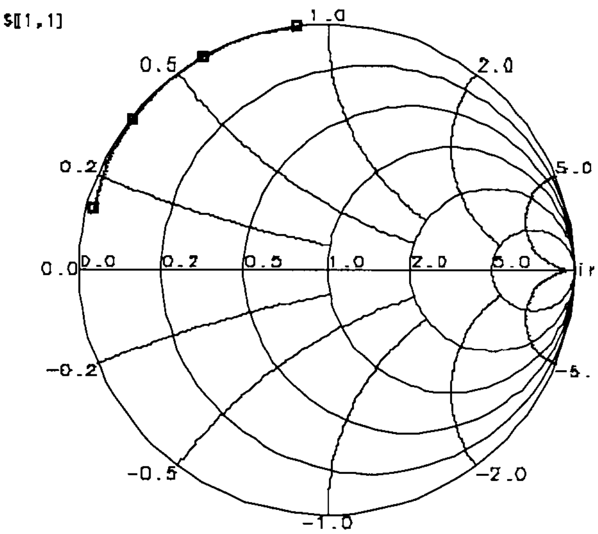


Fig. 6
Active inductor quality factor (left axis) and equivalent inductance in nH (right axis).



Frequency 15.0 ta 30.0 GH_z

Fig. 7
Active inductor frequency behaviour

In Fig. 6 is reported, on the right axis, the equivalent value of the inductance (L=O.2nH) and, on the left axis. the corresponding Q, that results to be in excess of 1000 over a relatively wide frequency range. Making reference to the notation used in Fig. 3, the equivalent inductance is:

$$L_{eq} = L_s - \frac{1}{\omega^2 C_s}$$

This inductance has a fairly constant value slowly growing with frequency due to the effect of Cs.

In Fig. 7 is reported the inductance as a function of frequency on the Smith chart.

The linearity and distortion of the active inductor was evaluated feeding a fixed frequency 25 GHz signal to the active inductor and measuring the reflected fundamental and second harmonic power components [l]. The input signal was swept in the range —40 ¸ +20 dBm, as reported in Fig. 8. The 1 dB compression point is about 16 dBm with a second harmonic ratio of -25dB.

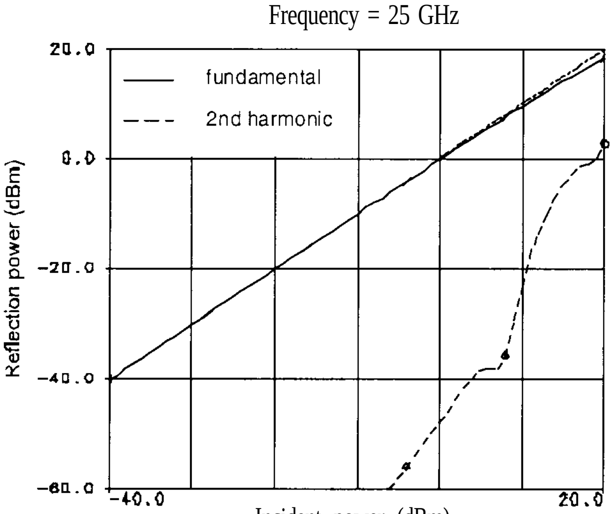


Fig. 8
Active inductor linearity and distortion.

V. CONCLUSIONS

A novel topology for grounded active inductor has been presented, based on a very simple application of the Miller's theorem. The basic circuit is composed by a single active device loaded by a narrow transmission line. The scheme is featured by extremely reduced and controllable losses, resulting in excellent quality factors. reduced size and low dissipation. A simple implementation of the circuit including bias circuitry has been performed in PHEMT monolithic technology, whose simulation results confirm the proposed approach.

VI. REFERENCES

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