A Fully Integrated Dual-Frequency Push-Push VCO for Wideband Wireless Applications

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Abstract — A fully integrated dual-frequency VCO providing not only a high frequency LO signal to transceiver mixers but also a half-LO-frequency signal to a PLL is described. The circuit has 1.2 GHz tuning range at 7 GHz, 25-dB suppression of fundamental-frequency (3.5-GHz) signal at 7-GHz port, and more than 20dB suppression of 7-GHz-signal at 3.5-GHz port. The VCO chip was packaged and resembled on board for phase-noise measurement. A phase noise of –80 dBc/Hz at 100kHz offset frequency was obtained. This work avoids the use of frequency dividers, hence the chip sizes, power consumption and cost are reduced.

I. INTRODUCTION

The advent of wireless communications has fueled a demand for low cost, high performance integrated circuits. Fully integrated RF transceivers are a common interest. A transceiver chip is more and more preferably to contain a local oscillator (LO) which provides local signal not only to the transceiver but also to an off-chip PLL. However, the available phase-locked loop (PLL) in product market mostly cannot handle a LO frequency higher than 4 GHz. For a LO frequency much higher than 4 GHz an extra frequency divider is always required. Another conventional solution is to multiply a LO signal at lower frequency acceptable by a commercial PLL using a doubler or a tripler and feed into the transceiver. Both cases, however, cause extra chip area and power consumption. The signal with either divided or multiplied frequencies has extra phase noise added by the frequency divider or multiplier. In addition, more design uncertainty is associated with more circuit blocks. Another technical drawback of the fundamental LO is that the low *Q*-factors at high frequencies will severely limit the phase-noise performance of a LO.

On the other hand, interest on wideband integrated LO covering desired frequency ranges in order to significantly cut down the cost of a communication system is also increasing. A typical solution is to have a single VCO that operates in different frequency ranges [1]. This, however, increases the design complexity. Although ring oscillators can provide multi-range frequency due to its tuning ability for wide frequency range [1], their highest operation frequencies and phase-noise performance at GHz range are limited.

This paper describes a single push-push VCO circuit for wideband wireless application, which provides not only a high frequency LO signal to transceiver mixers but also a half-LO-frequency signal to a PLL. This avoids the use of frequency dividers hence reduces chip size, power consumption and cost. The design is based on a 0.5-μm GaAs PHEMT technology with 25-GHz f_T.

II. PRINCIPLE OF A SINGLE FREQUENCY PUSH-PUSH OSCILLATOR

Push-push topology has been employed through the years [2,3,4,5]. They were realized based on distributed components, mostly in millimeter-wave frequencies. The block diagram of a single-frequency push-push circuit is given in Fig. 1.

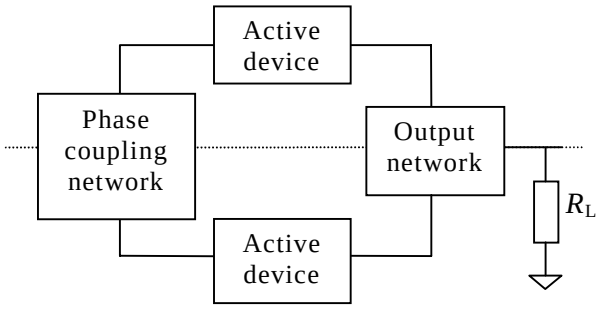


Fig. 1. Principle of a push-push oscillator

A push-push VCO is a balanced circuit containing two identical and symmetric circuits. The phase coupling network is for even-mode

suppression. The second-harmonic signal can be coupled from a virtual-ground node to the load (R_L), therefore double of the fundamental-frequency signal is obtain. The phase-coupling network and output network were mostly realized using distributed components, which is strongly influenced by operating frequencies.

III. CIRCUIT DESIGN OF THIS WORK

The circuit diagram of this work based on Colpitts structure is shown in Figure 2. The active devices FET_1 and FET_2 are biased with constant current sources I_1 and I_2, respectively. The circuit works at its fundamental frequency ($f_o/2$) determined by the two identical tanks (TANK A and TANK B). Even harmonic signals at nf_o (n=1, 2, 3, …) can be generated in phase at a fundamental virtual-ground node, which doubles the frequency range and introduces high loaded Q (Q_L). This improves the load pulling performance and phase noise. Fundamental signal $f_o/2$ can be coupled to off-chip PLL directly from a differential-node pair in the circuit, which simplifies the system architecture, (*e.g.* no need for an extra divided-by-2 prescalar), reduces current consumption and chip size.

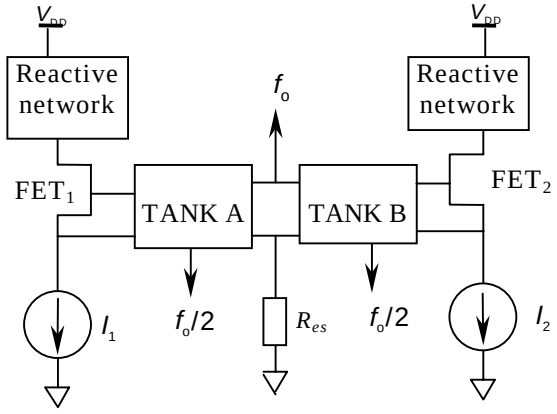


Fig. 2. A push-push VCO diagram

For wideband oscillators another requirement is to keep a constant loop gain over the whole frequency range. For this purpose the drains are connected via a reactive network instead of directly to the power supply. This network is designed to compensate a down-slipping loop gain at the higher end of the desired frequency band. Since they are apart from the tanks, the requirement of their absolute high Q is not critical.

Two identical LC tanks (Fig. 3) are designed at the fundamental frequency $f_o/2$. Due to the technology-related limitation in metalization thickness wide strips were chosen to enhance the Q of the inductors. In order to have a wider frequency tuning range, two variable capacitors are introduced in the tank. Even mode suppression is realized by a resistor R_{es} connected to a fundamental virtual-ground node, therefore no even mode oscillations at fundamental frequency can occur.

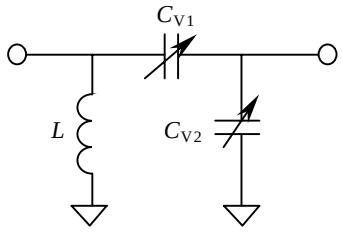


Fig. 3 A tank resonating at fundamental frequency

A block diagram of the complete VCO is shown in Figure 4. The described core VCO is followed by a buffer "*A*" to feed the PLL working at $f_o/2$, and buffers "*B*" and "*C*" working at f_o for transmitter (Tx) and receiver (Rx) mixers, respectively. Buffer "*A*" weakly couples a differential signal at $f_o/2$, amplifies it, then gives a single-ended output signal at the same frequency to a 50 Ω load. Its simplified schematic is shown in Fig. 5(a). Buffers "*B*" and "*C*" transfer a single-ended signal at f_o to two identical differential signals at the same frequency to the transceiver mixers, therefore should be optimized to realize on-chip matching to the Tx- and Rx- mixer input impedance, respectively. Their simplified schematic is shown in Fig. 5(b). Careful circuit design considerations such as tuned loads and variation compensation are incorporated to improve the output voltage swing and headroom of the buffers under the low supply voltage. A high-pass LC filter is inserted between the core VCO and the mixer buffers in order to suppress the leakage of $f_o/2$ signal resulted from practical asymmetry of the circuit due to process variation.

The circuit was designed to operate at frequency (f_o) of 7 GHz with 1.20 GHz tuning range including extra margin in frequency range in order to cover the frequency drift from desired due to process variation which can tremendously lower a yield.

In order to achieve high performance with low cost the circuits were designed into the Philips 0.5 μm gate length GaAs PHEMT process with 25 -GHz f_T.

The supply voltage V_{DD} was chosen to be 3.3 V for mobile operation.

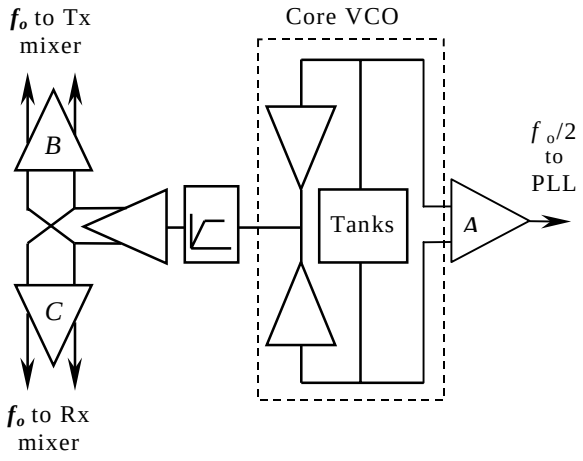
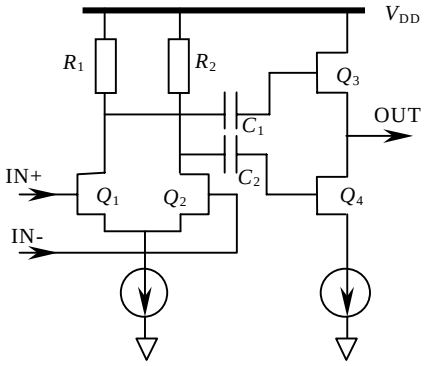
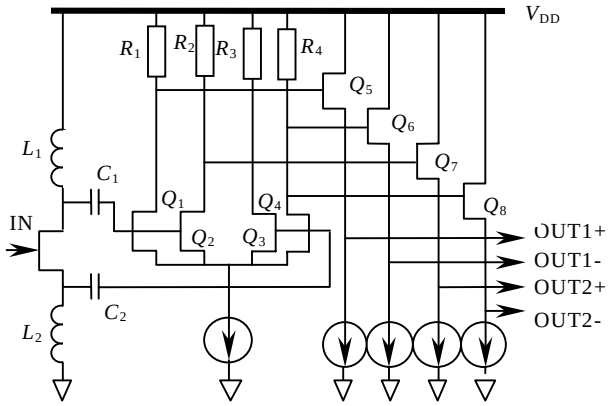


Fig. 4. Complete VCO



(a)



(b)

Fig. 5 LO buffers (a) differential-to-single-ended at f_o /2 and (b) single-ended-to-differential at f_o

IV. MEASUREMENT

On-wafer measurements under a temperature of 30°C and 80°C were carried out. During the measurement an external control voltage is used to compensate I_{dss} variation. The measured frequency (f_o) vs. tuning voltage of core VCOs is shown in Fig. 6. The circuit has more than 1.2 GHz tuning range. The bigger difference of the frequency vs. tuning voltage curve observed at around V_{tune} =0.5~0.9 V between simulation and measurement is due to the unexpected shift of the C_v~V_{tune} corner of the variable capacitance along the X-axis. The simulation gave very good prediction in output power to PLL, as displayed in Fig. 7. The other two buffers, "*B*" and "*C*", however, consume more current (>10 mA) than simulated for the same power level to the mixers. Measurement shows 25-dB suppression of fundamental frequency (3.5-GHz) signal at 7-GHz port, and more than 20dB suppression of 7-GHz signal at 3.5-GHz port.

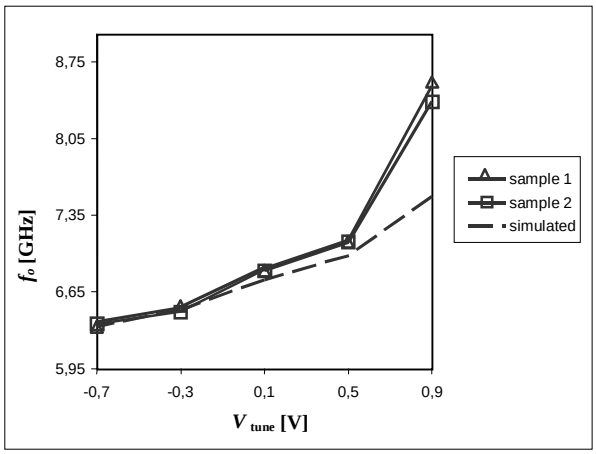


Fig. 6. Measured frequency vs V_{tune}

The core VCO and the buffers consume 10 mA and 25 mA, respectively. Although the circuit was designed to operate with a 3.3 V, it performs within a wide range of supply voltage (1.8~3.8V). A photograph of the complete VCO for testing is given in Fig. 8. The size of this test block is 2.0x1.75 mm ^{2}.

The complete VCO has been packaged and resembled on-board together with a PLL. The packaged VCO locked by the PLL was measured on board in order to obtain the phase-noise performance. On-board efforts were made to get rid of unwanted board-level coupling. No unexpected phenomenon caused by the package was observed compared to the bare-die on-wafer measurements. The measured VCO phase noise is

–80 dBc/Hz at 100kHz offset frequency from the carrier.

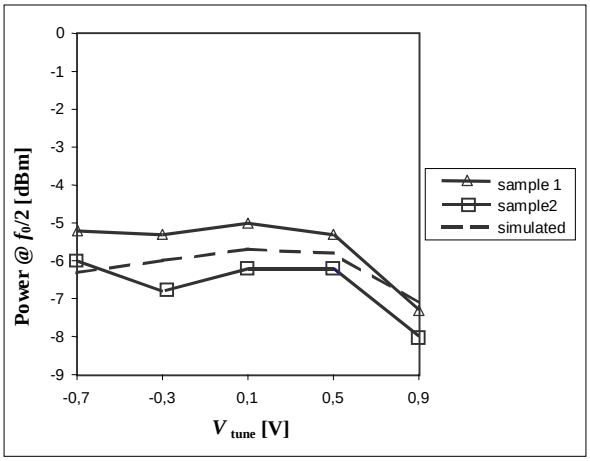


Fig. 7. Measured output power to PLL vs V_{tune}

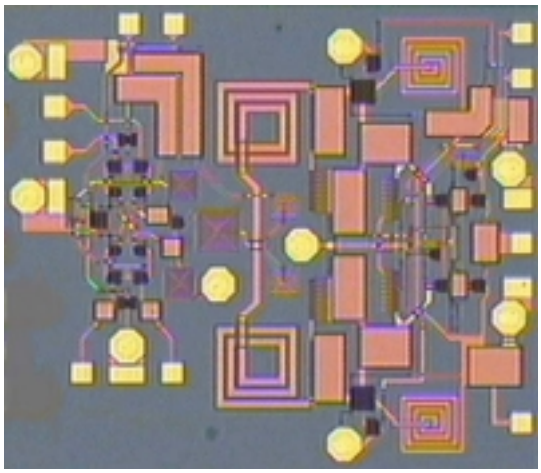


Fig. 8. A photograph of the VCO with buffers for testing.

V. CONCLUSIONS

The design and measurement of a fully integrated VCO based on a 0.5-µm GaAs PHEMT technology with dual frequencies at 3.5 and 7 GHz are described. Good agreement between simulation and measurement was obtained. The circuit provides output signals not only to transceiver mixers at 7 GHz but also to an off-chip PLL at 3.5 GHz. This avoids the use of frequency dividers, hence the chip sizes, power consumption and cost are reduced. A 25-dB suppression of fundamental frequency (3.5 GHz) signal at 7-GHz port, and more than 20dB suppression of 7-GHz signal at 3.5-GHz port were obtained. The VCO has a very wide frequency tuning range but still shows a good phase noise of –80 dBc/Hz at 100kHz offset frequency from the carrier. To our knowledge, this is the first reported packaged VCO chip working at this frequency for wireless applications. The VCO is suitable for wideband or multi-band wireless networks. The dual-frequency technique used in this work is also applicable to other frequency bands.

VI. ACKNOWLEDGEMENT

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