# Characterization of an ASIC Front-End electronics dedicated to Silicon Drift Detectors

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## The Context

Large-area multi-anode Silicon Drift Detectors (SDDs) have X-ray imaging and spectroscopic characteristics that make them extremely attractive in the perspective of their applications to the field of space astrophysics and in instruments for medical diagnostic imaging.

We describe here the activity aimed to develop an ASIC suitable for coupling with SDDs.

The ASIC described here is the first prototype of front end electronics to be used for the readout of large-area SDD of a similar design of that one developed for the Inner Tracking System (ITS) in the ALICE experiment of the Large Hadron Collider (LHC) at CERN.

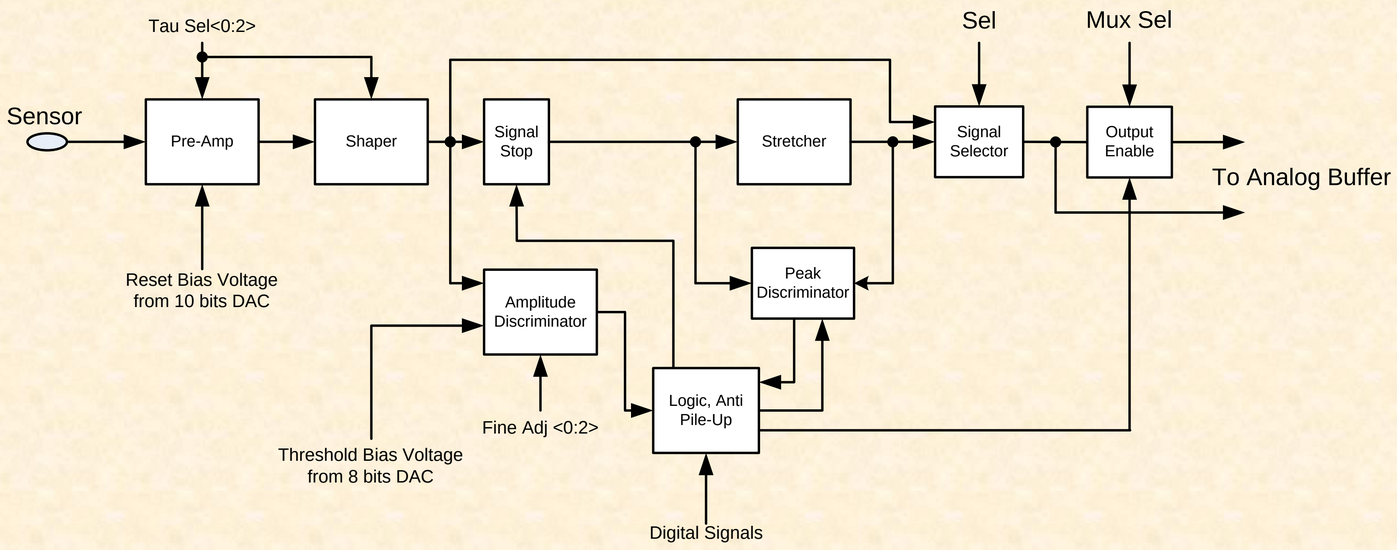
These detectors can reach large area of some tenth of $cm^2$ with anode pitch of various size from some hundred of micrometer so a millimeter, and can be used with very good spectroscopic capabilities for low energy X-ray detection.

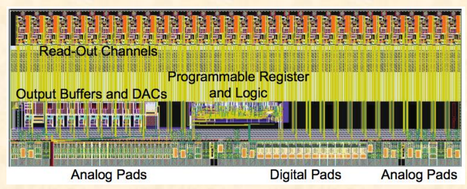
Similar detector with their electronic readout can find application in many different mission ranging from configuration devoted to X-ray spectroscopy, imaging or timing observation to configuration conceived for gamma-ray observation like for example in architectures at the base of a Compton telescope design.

## ASIC Main Features

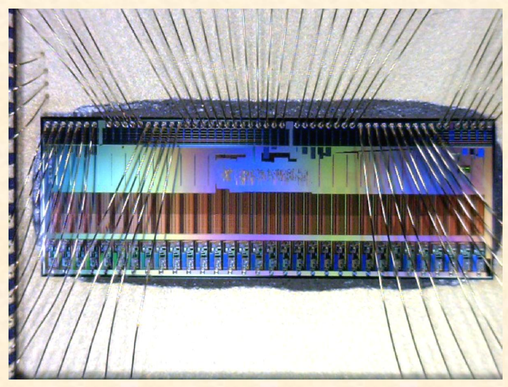
| FUNCTION | IMPLEMENTATION |
|---|---|
| Input: Readout of 32 SDD anodes | 32 parallel inputs channels, current input<br>Channel pitch 200 μm |
| Pre-amp | DC coupling<br>Input range 120 – 12000 $e^-$<br>Detector param. 150 pA max leak curr, 0.5 pF max |
| Signal processing<br>32 Read-out Pixel Cell (RPC) | Low-noise preamplifier<br>Pulse shaper CR-$RC^2$ with pole zero suppression,<br>Amplitude discriminator<br>Peak discriminator and stretcher<br>Digital circuits required for cell operation |
| Commanding<br>configuring the internal registers | Shaping time (selectable from 0.5 to 10 μsec)<br>Discriminator level (general + individual tuning of the ch)<br>Channel disabling (of both pre-amp and discriminator)<br>External trigger (selectable)<br>Output mode: shaper or stretched output in selected ch |
| Output | Internal trigger (OR of all channel trigger)<br>Analogue output (parallel) for ch from #15 to #22<br>Analogue output (serial) of stretched signals after a MUX |

## One channel simplified architecture




The first ASIC prototype design



The ASIC in its packaged version

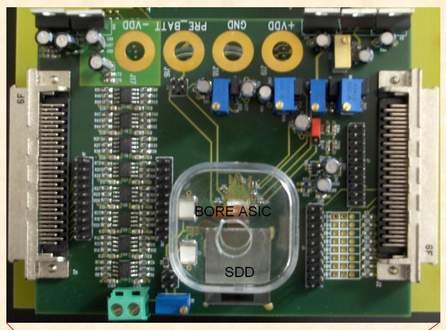
0.35 mm CMOS technology

Die dimension are 6.4 x 2.3 mm channel pitch 200 μm

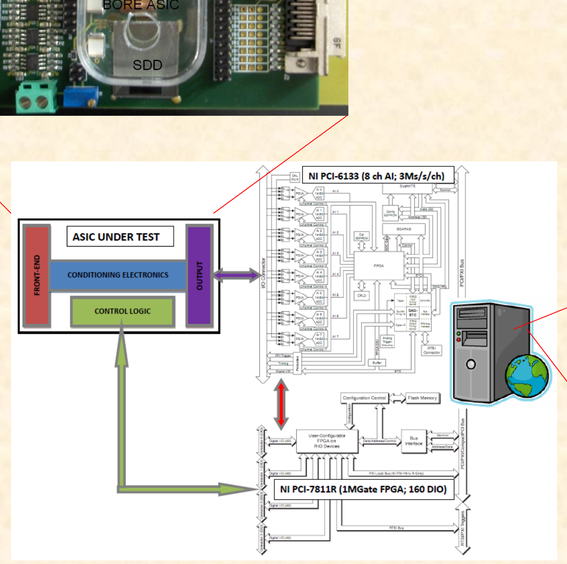
## The testing system

The ASIC testing system consist of two PC boards: the first one with digital input/output for ASIC configuration and commanding, the second one for ASIC commanding during operation and for ADC conversion.

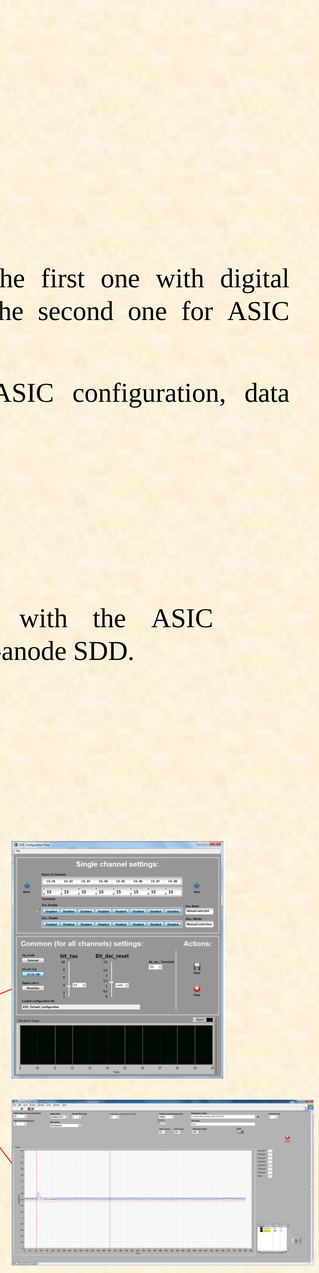
Different graphical interfaces are used for choosing ASIC configuration, data acquisition and visualisation




Prototype board with the ASIC bonded to a multi-anode SDD.

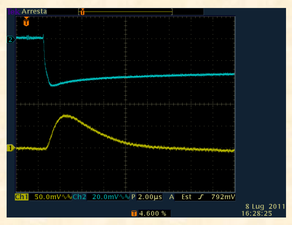


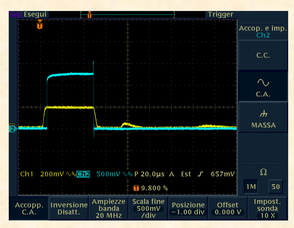

Schematics of the ASIC Test Equipment.

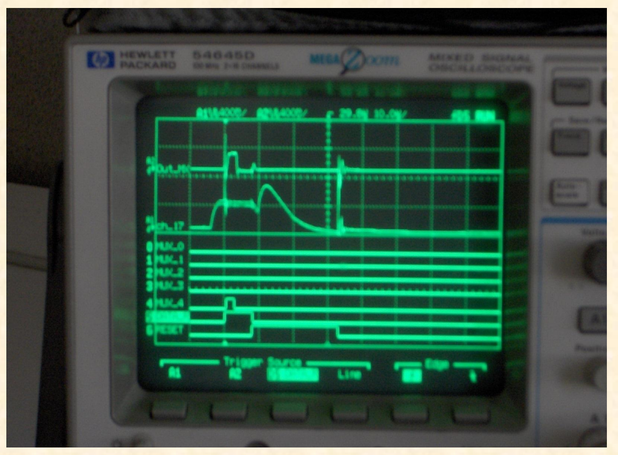



Graphical interfaces of the Test Equipment for ASIC configuration and real time signals display

## Read out sequence for a detected event







ASIC functionality on ch #15 (ch #15 chain ON (shaping 1 μsec), all other channels OFF)

Left: Output of the channel chain from the tes_pin of the channel (available only for ch from #15 to #22 will be removed in final design). Top ASIC in shaping configuration, bottom ASIC in stretching configuration, in both cases internal trigger is used.

Right: Output from the MUX pin (internal trigger is used); signal sequence from top to bottom

| | |
|---|---|
| Out from ch #15 chain | Analog |
| Out from MUX | Analog |
| Input MUX address | Digital (5 bits) |
| Input Sample | Digital (must be long enough to allow multplexing operations) |
| Input Reset | Digital |

The functional behaviour of the ASIC is correct; the performance figure of the ASIC are still under test, expectation from circuit simulation are that the noise figure is contained in some tent of e- rms, with a power consumption of about 1 mW/ch

A new ASIC run is foreseen in the next months