ALTERNATIVE ARCHITECTURES OF SOI MOSFET FOR IMPROVING DC AND MICROWAVE CHARACTERISTICS

M. Dehan, D. Vanhoenacker and J.-P. Raskin

Microwave Laboratory, Université catholique de Louvain
Place du Levant, 3, B-1348 Louvain-la-Neuve, BELGIUM
e-mail: raskin@emic.ucl.ac.be

ABSTRACT

DC and high frequency characteristics of innovative SOI MOSFET's such as graded channel and dynamic threshold voltage MOS are presented in this paper. These architectures are very promising for high frequency low power low voltage analog applications.

I. INTRODUCTION

The boom of mobile communications leads an increasing request of low cost and low power mixed mode integrated circuits. Maturity of silicon-based technology and recent progresses of MOSFET's microwave performances [1], explain silicon success as compared to III-V technologies. Silicon-on-Insulator (SOI) based MOSFET's are very promising devices for multigigahertz applications. Thin-film SOI MOSFET's offer indeed interesting low-voltage performances, higher speed and increased integration density, all with simpler processing than bulk silicon MOSFET's of comparable size [2]. Many recent realizations of logic circuits, memories, and RF circuits [3] have confirmed both the advantages and the viability of thin-film SOI circuits, even in the case of very large systems. Moreover, the scaling down process of CMOS devices which has started years ago and it is still improving their DC and high frequency characteristics and, of course, their compactness and power consumption. However, in few years, we are going to reach the limits of the classical photolithographic systems for defining precise and reliable submicrometer structures. In order to push those limits farther, novel architectures of MOSFET's have to be considered as an attractive solution. The DC and microwave performances of graded channel and dynamic threshold voltage MOSFET's are presented and compared to conventional Fully Depleted (FD) SOI nMOSFET's in this paper.

II. GRADED CHANNEL FD SOI MOS

Asymmetric doped channel MOSFET's have recently been investigated by several authors in bulk [4] and SOI technologies as a possible solution for the problems of premature drain break-down, hot carrier effects, and threshold voltage (V_{th}) roll-off issues in deep sub-micrometer devices. In these works, the doping of the channel region is performed by a tilted ion implantation in the source side after the gate formation. Recently, Pavanello *et al.* in [5] have presented a new asymmetrically doped body device, called the graded-channel SOI nMOSFET (GC) shown in Fig. 1. The asymmetric doping profile was obtained by varying the position of the V_{th} implant along the channel, preserving the body region near the drain at natural wafer doping. Contrary to previous reports, the GC SOI processing is fully compatible with the conventional FD SOI MOSFET process flow, with no additional steps needed. Similar to a DMOS [6], the device can be viewed as two sub-devices connected in series: an enhancement mode device at the source side, and a depletion mode device at the drain side, each has a different V_{th} and "channel" length. The effective channel length (L_{eff}), when the device is on, is mainly determined by the GC region, which is much shorter than the physical gate length. As the result, for the same physical gate length, the GC device can provide higher drive current, higher peak transconductance, higher output resistance than a conventional CMOS device with Uniformly Doped (UD) channel, resulting in a high performance device with high cut-off frequency and high gain as demonstrated later.

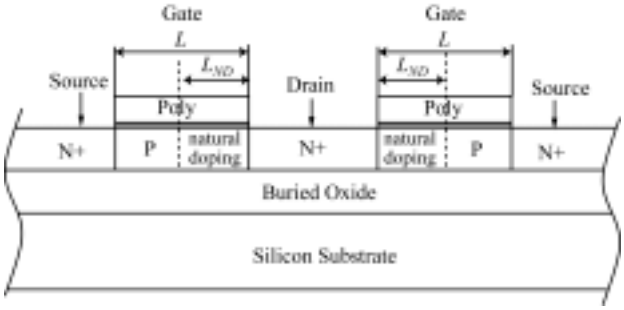


Fig. 1. Cross-section of interdigitized graded channel SOI nMOSFET's.

The thicknesses of the gate oxide, silicon film, and buried oxide were 30, 80, and 390 nm, respectively, and channel doping level (implanted region close to the source) was approximately equal to 10^{17} cm^{-3}, resulting in a threshold voltage of 0.3 V.

The MOSFET's to be characterized at high frequencies are embedded in a coplanar waveguide (CPW) structure designed to minimize the ground inductance. Using standards implemented on the SOI wafer, a through-reflect-line (TRL) calibration is performed. As a results, the reference planes are positioned close to the device, effectively reducing the input and output capacitances. More details about the calibration and de-embedding procedure can be found in [7], [8].

The drain current (I_{DS}) is measured as a function of drain voltage (V_{DS}) and for various gate voltage (V_{GS}), for both UD and GC devices (Fig. 2). Comparing devices with almost identical effective channel length, i.e., UD with L = 1 µm and GC with L = 2 µm and L_{ND}/L = 0.5, and UD

with L = 0.6 µm and GC with L = 1 µm and L_{ND}/L = 0.5, it is clear that the GC configuration exhibits superior output characteristics, improving not only the saturation current but the parasitic floating-substrate effects as well. The premature breakdown voltage is increased, whereas the extremely flat saturation current exhibited by the SOI GC, presenting almost zero slope, indicates a tremendous improvement in the output conductance. Actually, the GC MOS transistor can be seen and analyzed as two FD SOI MOS sub-transistors connected in series, one for the P-type doped region and one for the undoped channel region, the gate of these two sub-transistors being connected together. Considering a simplified small-signal equivalent circuit, we demonstrate that the output conductance (G_d) of the GC MOS is given by:

$$G_d = \frac{G_{d1}G_{d2}}{G_{m2}} \qquad (1)$$

where G_{d1}, G_{d2} and G_{m2} are, respectively, the output conductance of the FD SOI MOS transistor modeling the P-type doped channel region, the output conductance and the gate transconductance of the FD SOI MOS transistor modeling the undoped channel region. The output conductance of the GC MOS shows a similar expression than the well-known cascoded transistors topology. Thanks to the equivalent gate transconductance of the equivalent undoped FD SOI MOS sub-transistor the global output conductance of the GC MOS is greatly reduced.

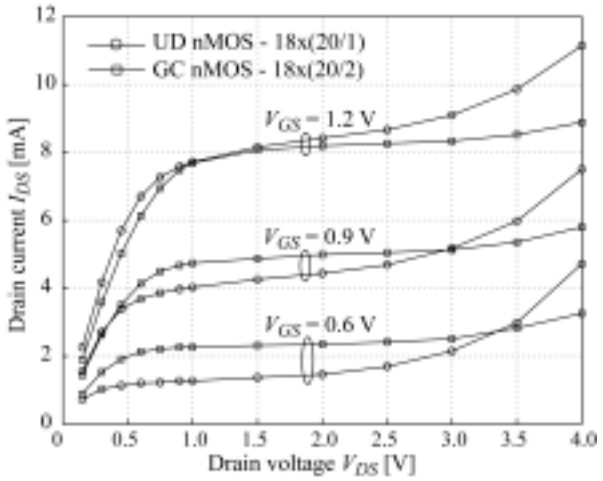


Fig. 2. Measured I_{DS} versus V_{DS} curves for GC and UD SOI nMOSFET's.

From Fig. 2 we extracted the Early Voltages (V_{EA}) of the GC's with similar effective channel than the UD devices (Table I), defining V_{EA} by the linear regression of the I_{DS}-V_{DS} curve in the internal 1.5 V < V_{DS} < 2.5 V. A great improvement in the Early Voltage of the GC devices is obtained due to the reduced channel length modulation provided by the presence of a strong depletion at the undoped region which is especially interesting in mixed analog-digital applications. Also shown in Fig. 2 is the ratio of the drain breakdown voltage for GC and UD transistors. For each effective channel lengths and V_{GS} the breakdown voltage of GC's is always larger than that for conventional UD's. No particular degradation of the subthreshold swing has been observed with GC MOS transistors. Effectively, it appears that GC and UD with same effective channel length present similar subthreshold voltage as shown in Table I.

Fig. 3 presents the simulated longitudinal electric field in the thin silicon film for a 2 µm GC MOS (L_{ND}/L = 0.5) and 1 µm UD MOS under V_{GS} = 0.6 V and V_{DS} = 0, 0.4 and 1 V. The simulations have been performed with the commercial 2-D numerical simulator SILVACO [9]. The distribution of the longitudinal electric field in the doped and undoped regions of the GC MOS is clearly shown. Comparing the longitudinal electric field for UD and GC MOSFET's of same effective channel length, an important reduction of the peak electric field at the drain side is achieved with GC MOS. This reduction of longitudinal electric field means lower impact ionization, hot electron degradation as well as higher breakdown voltage.

	f_T [GHz]	f_{max} [GHz]	V_{EA} [V]	S [mV/dec]
UD 2 µm	2	4.8	- 28	65
UD 1 µm	5.7	13	- 13	68
UD 0.6 µm	8.4	22	- 9	75
GC 2 µm	4.1	10.5	- 105	66
GC 1 µm	9.0	20.5	- 42	73

Table I. Extracted Early voltages (V_{EA}), subthreshold swing (S), f_T and f_{max} for GC and UD SOI nMOSFET's.

Cutoff frequencies are given at V_{GS} = 1 V and V_{DS} = 2 V. Comparing the cutoff frequencies for UD and GC SOI nMOS with the same drawn gate length (L = 1 µm), the interest of asymmetric doped channel for high frequency applications appears clearly. The improvement provided by the GC device (with L = 1 µm and L_{ND}/L = 0.5) reaches approximately 55 % for f_T and f_{max}, these cutoff frequency values are comparable to those obtained for a UD device with L = 0.6 µm, as shown in Table I. The increase of cutoff frequencies for GC devices is due to the artificial reduction of the effective gate length as explained previously.

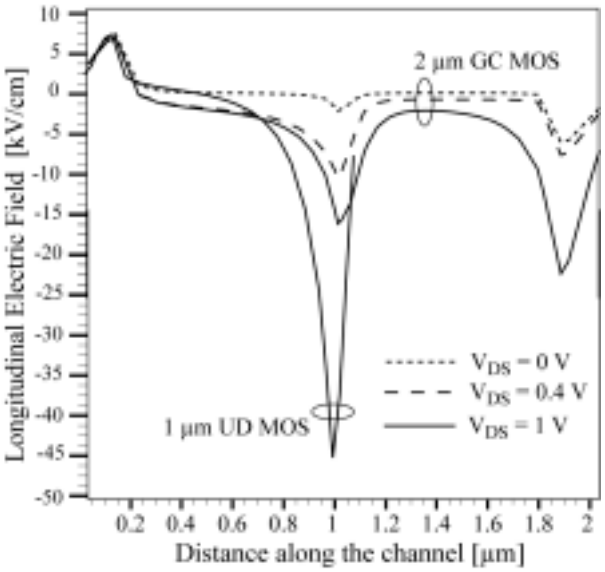


Fig. 3. Longitudinal electric field in the thin silicon film for a 2 µm GC MOS (L_{ND}/L = 0.5) and 1 µm UD MOS under V_{GS} = 0.6 V and V_{DS} = 0, 0.4 and 1 V.

Table II represents the comparison of the equivalent circuit lumped elements for UD and GC nMOSFET's with same drawn channel length (L_{drawn}). It demonstrates that thanks to the reduction of the effective channel length, higher cutoff frequencies and lower output conductance are achieved without agressively reducing the physical channel length of the MOS transistor. GC MOS technology described here is fully compatible with mainstream CMOS technology.

UD nMOS	GC nMOS - L_{LD}/L = 0.5
L_{drawn} = 2 µm	L_{drawn} = 2 µm
L_{eff} = 1.9 µm	1 µm
G_m	Higher (~30 %)
G_d	Lower (G_d/10…50)
C_{gs}	Lower (~50 %)
C_{gd}	Slightly higher
R_{ge}	Similar
R_{se}	Similar
f_T	Higher (~2 times)
f_{max}	Higher (~2 times)

Table II. Comparison of equivalent circuit lumped elements for UD and GC MOS with same drawn channel length.

One drawback of the GC MOS structure is the possible misalignment of the mask used to protect the GC channel region from V_{th} implant. The misalignment of this mask will lead to a higher or lower value of L_{ND}/L and then a higher or lower L_{eff} than expected. The electrical characteristics of MOS transistor being strongly linked to the effective channel length, higher dispersion of transistor characteristics can be expected with GC MOS. But at the other hand, we have to keep in mind that most of the time analog transistors are composed of several gate fingers connected in parallel to each other as shown in Fig. 1. Multi-fingers structure is usually required to reach the optimum *W/L*, high saturation current, low gate resistance, good microwave performance, etc. This multi-fingers scheme leads to a reduction of the misalignment troubles of the GC-mask. Actually, if we consider for example a misalignment of 10 % for a drawn gate length of 1 µm, we will have individual transistors with alternatively effective channel length of 0.4 and 0.6 µm, instead of 0.5 µm for each if we had really obtained L_{ND}/L = 0.5. Using 2-D numerical software SILVACO we have simulated the drain current versus gate and drain voltages for the case of a perfect alignment (L_{ND}/L = 0.5, only transistors of L_{eff} = 0.5 µm) and the case considering a misalignment of 0.1 µm (identical number of transistors with L_{ND}/L = 0.4 (L_{eff} = 0.4 µm) and L_{ND}/L = 0.6 (L_{eff} = 0.6 µm) due to the multi-finger structure). The results show an increase of the saturation drain current of less than 10 % for the multi-finger transistors for which a GC-mask misalignment of 0.1 µm is considered. This dispersion is not unusual and can be overcome by classical tuning techniques.

III. DYNAMIC THRESHOLD VOLTAGE SOI MOS

The dynamic threshold voltage MOS is a MOS transistor for which the gate and the body channel are tied together. Fig. 4 shows the structures of conventional and DT MOSFET's. All DTMOS electrical properties can be deduced from standard MOS theory by introducing V_{BS} = V_{GS}. The main advantage of DTMOS over conventional MOS is its higher drive current at low bias conditions. To keep the body to source current as low as possible, the body bias voltage must be kept lower than 0.7 V. It seems obvious that the DTMOS transistor is an attractive component for low voltage applications. But as shown in Fig. 4, its 3-D architecture is much more complex than the conventional MOS. It results in an increase of the extrinsic parasitic components which can degrade the microwave characteristics.

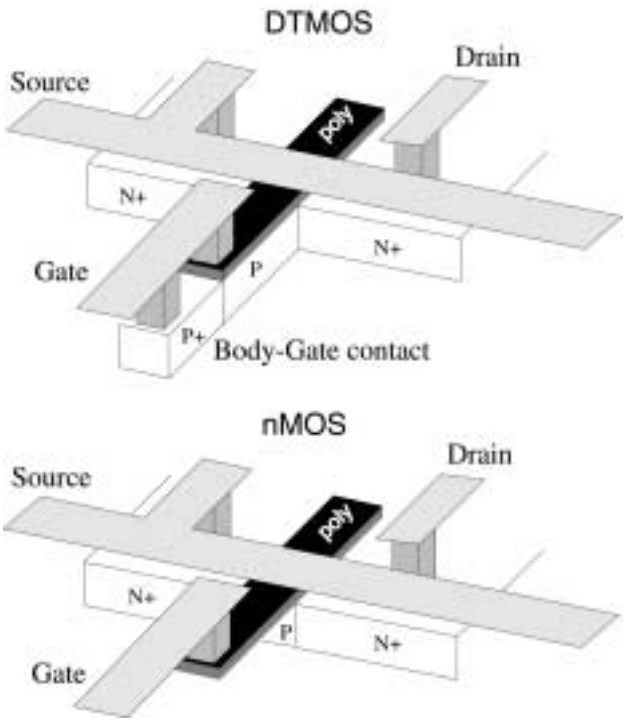
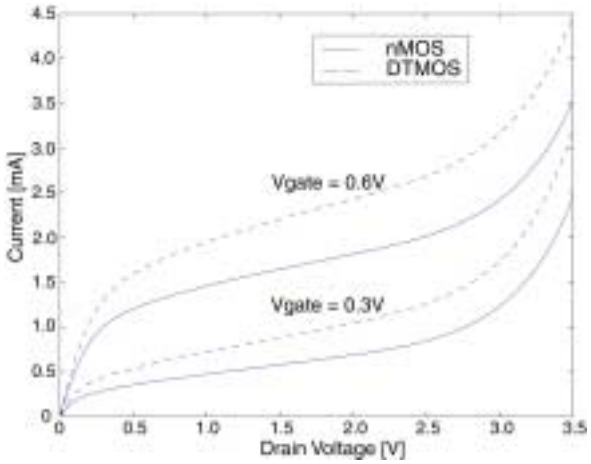


Fig. 4. 3-D architectures of SOI DTMOS and nMOS.

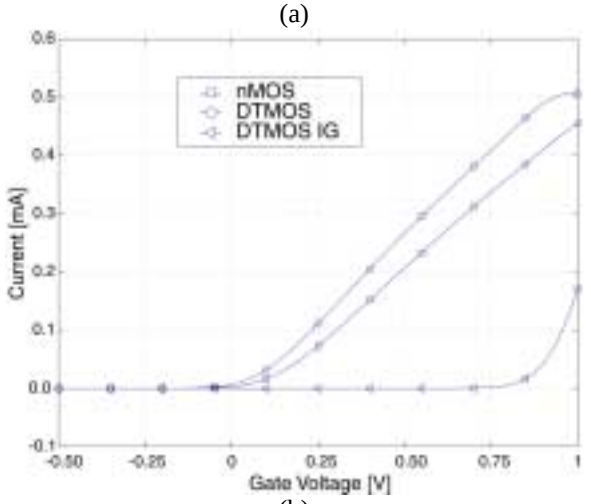
SOI DTMOS and FD SOI MOS composed of 8 fingers of 12 µm each and channel length of 1 µm have been compared. Fig. 5 presents the I_{DS}-V_{DS} and I_{DS}-V_{GS} curves for both devices. As predicted, the DTMOS exhibits a higher current drive capability and lower threshold voltage. The slope of the I_{DS}-V_{GS} curve in Fig. 5b for the DTMOS is slightly higher than its of the FD SOI nMOS, this means an increase of the gate transconductance. When the gate voltage is raised above 0.7 V, the gate/body to source and the gate/body to drain current increase, and the total drain current is reduced (Fig. 5b).

The magnitude of the S-parameters, current gain (H21) and Maximum Available Gain (MAG) are presented in Fig. 6 under V_{DS} = 1 V with V_{GS} = 0.6 V and 1 V, respectively for DTMOS and FD SOI nMOS. The DTMOS presents a higher $|S_{21}|$, and due to the increase of extrinsic capacitances and resistances related to its more complex structure, $|S_{11}|$ and $|S_{22}|$ are slightly lower. Nevertheless, SOI DTMOS exhibits similar MAG and

cut-off frequencies than FD SOI MOS under lower bias conditions.

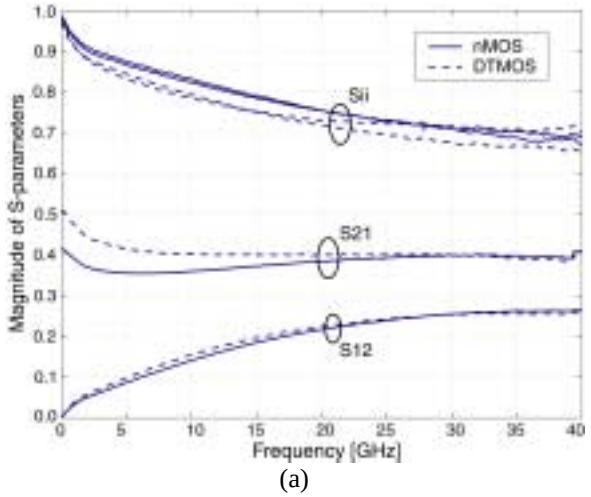


(a)

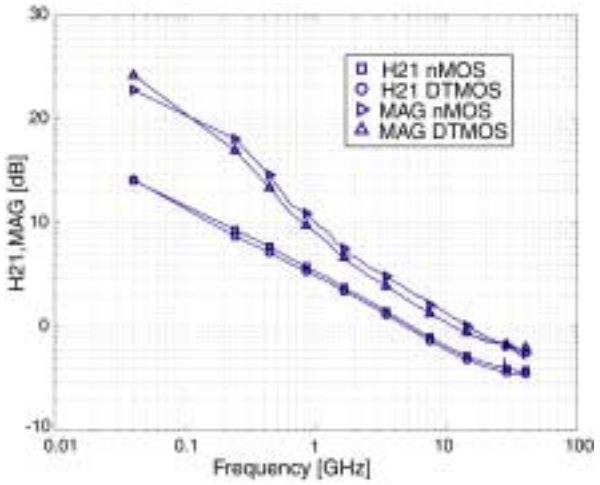


(b)

Fig. 5. I_{DS}-V_{DS} (a) and I_{DS}-V_{GS} (b) curves for SOI DTMOS and nMOS.



(a)



(b)

Fig. 6. S-parameters, H21 and MAG vs. frequency for SOI DTMOS and nMOS.

IV. CONCLUSION

DT and GC SOI MOSFET technologies described here are fully compatible with mainstream CMOS technology and demonstrate improved performances such as lower output conductance, higher drive current and high cut-off frequencies at low voltage low power conditions without aggressively pushing the technology through device scaling to reduce cost.

V. REFERENCES

[1] C. Raynaud *et al.*, *Proceedings 1998 IEEE International SOI Conference*, October 1998, pp. 67-68.

[2] J.-P. Colinge, "Silicon-on-Insulator technology: material to VLSI", Boston – Dordrecht – London: Kluwer Academic Publishers, 1991.

[3] M. Goffioul *et al.*, *30th European Microwave Week proceedings EuMC'2000 and GAAS'2000*, Paris, France, October 2-6, 2000, pp. 407-410.

[4] S. Odanaka and A. Hiroki, *IEEE Trans. Electron Devices*, vol. 44, pp. 595-599, April 1997.

[5] M. A. Pavanello *et al.*, *Electrochemical and Solid-State Letters*, 3 (1) 50-52, pp. 50-52, 2000.

[6] M. Hong, *IEEE Transactions on Electron Devices*, vol. 40, pp. 2222-2230, Dec. 1993.

[7] R. Gillon *et al.*, *26th European Microwave Conference proceedings EuMC '96*, Prague, Czech Republic, September 9-12, 1996, pp. 170-173.

[8] J.-P. Raskin *et al.*, *IEEE Transactions on Electron Devices*, vol. ED-45, no. 5, pp. 1017-1025, May 1998.

[9] SILVACO International Software, Santa Clara, CA, USA, 2000.