SIZE DEPENDENT INFLUENCE OF THE PAD AND GATE PARASITIC ELEMENTS TO THE MICROWAVE AND NOISE PERFORMANCE OF THE 0.35 μm n AND p TYPE MOSFETs.

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ABSTRACT

Noise and s-parameters of the p and n type MOSFETs were measured and simulated for the different bias points. The pad parasitic models of the „short" and „open" were extracted by means of comparison of measured and simulated s-parameters. The influence of the pad elements on the microwave noise was analyzed. The simulation of intrinsic device noise was performed on the basis of good fit of measured and simulated noise and s-parameters of the DUT. For the narrow gate (50 μm) width devices the pad parasitics significantly affect microwave noise performance for both p and n type devices. At the lower drain currents the kinks and loops in the s-parameters were observed. At low drain current a resonant peak in NF_{min} and R_n around 8 GHz was found. Those resonant effects observed in noise and s-parameters diminish with the increase of the drain current and were qualitatively accounted for by the simulations by using equivalent circuit with the parasitic inductive element coupled to the gate.

INTRODUCTION

Submicron gate length MOSFETs are being more widely used in the digital and high performance analog circuits. Thus noise properties as the limiting sensitivity factor for analog applications of the device are of great importance. However, microwave noise together with *s*-parameters can serve as the powerful tool for the extraction of small signal and noise models [1,2]. For the scaled down devices the influence of the pad parasitic elements is increasing and can affect the microwave performance of the device under test (DUT). Thus, it is important to resolve the noise sources originating from the pads and transistor itself. Moreover, the knowledge of the noise sources itself can support the development of the noise equations in the MOSFET compact models and predict the microwave performance of the device in the design process.

In this work we have investigated the influence of gate and pad parasitic elements on the microwave noise of submicron (L=0.35 μm) *n* and *p* type MOSFETs, fabricated on one wafer, with different gate widths [3].

DEVICES AND MEASUREMENT SETUP

The gate width (W), finger unit width (w), gate length (L), number of fingers (*No.*) and the best bias point are presented in the table 1. The best bias point in terms of gain/noise trade-off was determined from a number of noise and *s*-parameter measurements.

Table 1. The gate sizes of *n* and *p* type MOSFETs and the best bias point.

Device	type	L (μm)	W (μm)	*No.fing*	w (μm)	V_D (V)	V_G (V)	I_D (mA)
41/42/43	n	0.35	200/100/50	16/8/4	12.5	1.5/2.0/1.5	0.9/1.4/1.1	9.8/11/2.9
31/32/33	p	0.35	264/132/66	16/8/4	16.5	-1.5/-1.5/-1.5	-1.4/-1.9/-1.9	10/10/5.6

On-wafer microwave noise and scattering parameters were measured with ATN NP5 noise measuring system in the 2-26 GHz frequency band. Simulations were performed with EEsof MDS and Microwave Office version 3.22.

PAD PARASITIC MODEL

The pad parasitic model was extracted from the measured *s*-parameter of the „open" and „short" dummy patterns. The model parameters are presented in the table 2 and were kept fixed in further simulations for all devices on wafer. Measured and simulated *s*-parameters of dummy structures are presented in the fig.1. At high frequencies *s*-parameters of „open" and „short" deviates from the ideal model thus indicating of high loses at the input and output ports. L_{GP}, L_{SP}, L_{DP} are the parasitic gate, source and drain pad inductances. C_M, C_{M2} are capacitances between the signal and ground pads, C_{SUB}, C_{SUB2} are the capacitances between the top metal and substrate, C_T is the gate/drain capacitance. R_{DB}, R_{DB2} are the gate and drain pad/substrate resistances. The de-embedding of scattering parameters of pads free MOST [2] was performed using an improved de-embedding method [4] with both "open" and "short" patterns.

Table 2. Pad model parameters.

C_T fF	C_{SUB}, C_{SUB2} fF	R_{SUB},, R_{SUB2} Ω	C_M,, C_{M2} fF	L_{GP} pH	L_{SP} pH	L_{DP} pH
4.5	72	324	10	17	13	28

INFLUENCE OF GATE AND PAD PARASITICS TO THE NOISE AND *S*-PARAMETERS

The equivalent circuit elements L_G, L_S, L_D, R_G, C_{SB}, C_{DB}, R_{DB}, R_S are bias independent. The C_{GS} will increase with I_D by increasing V_G at fixed V_D, because the pinch-off point of the channel will move towards the drain. The complete small-signal model of the DUT was found by adding pad parasitic model to the pad-free MOSFETs model extracted in [2]. The bias dependent model parameters were found by using the same procedure but keeping the bias independent parameters fixed to the original values. The current gain cut-off frequency extracted from the model fitted well the experimental data. The model parameters and F_T for the *n* and *p* type transistors biased with the best bias point are presented in the table 3.

Table 3. The MOSFET model parameters obtained for the optimal bias points.

No	F_T GHz	R_G Ω	R_D Ω	R_S, Ω	R_{DS} Ω	R_{DB} Ω	g_m mS	C_{GD} fF	C_{GS} fF	C_{GB} fF	C_{DB} fF	C_{SB} fF	R_{DSB} Ω	R_{SB} Ω	L_G pH	L_S pH	L_D pH
41	30	4.69	1.5	16.7	233	0.08	57	50	61	99	71	84	225	0.25	9.3	23	15
42	30	6.39	1.9	16.8	477	6.4	29.8	23.4	60	51	40	4.7	228	3.47	8	36	12
43	25	12.6	2.4	8.3	1646	5.2	9	12	30	18	22	4.7	300	1.5	11	32	16
31	13	8.5	0.05	17	236	0.66	36	68	301	31	124	4.5	230	0.6	4.3	14	15
32	13	15.0	0.39	17.6	450	11.6	15.6	49	109	23	77	4.15	404	0.55	11	12	12
33	12	53.4	0.02	19	892	1.35	7.9	29	58.8	19.3	37.8	5.6	400	0.8	4.8	5	12

Measured and modeled *s*-parameters of the DUTs 41,42 and 43 for the best bias point (see table 1) are presented in the fig.4. We observe very good fit of simulated to measured results confirming that pad parasitic model is properly found. For the lower gate biases and thus lower drain currents (I_D<10 mA) the specific loops and kinks appear in *s*-parameters, see fig.5. Here the evolution of *s*-parameters upon the gate bias is given. The loops turn into the kinks and further on with the increase of the current they disappear. Note that for the *p* type devices the similar trend was observed. We have modeled *s*-parameters by using equivalent circuit described in [2] with additionally connected to the gate the bias dependent parasitic capacitance C_{sch} coupled to a 330 pH parasitic inductive element L_{par} (see fig.6). The origin of that inductance can be associated with the self and mutual inductance [5] of the gate stripes. Roughly evaluated total inductance for the 41 device is of 300 pH magnitude. The proposed equivalent circuit model qualitatively accounts for the measured data. The increase of the capacitance C_{sch} with the bias masks the influence of the inductance and thus the loops and kinks disappear. The observed kinks in *s*-parameters influence to the NF_{min}, see fig.7. The additional parasitics at the gate, that added to the previously extracted small-signal model [2], account well for the noise and *s*-parameters (fig.8,9,10) for all bias points including the best ones, where C_{sch} increases with bias and the influence of the parasitic inductance disappears, see fig.5,8. The noise resistance and optimum source reflection coefficient give very good fit too (see fig.9,10). The parasitic gate elements of the MOST might cause the resonant effects, which degrade RF and noise performance as well. We have observed recently very similar resonant effects for the 0.18μm gate length MOS transistors, fabricated in different factory, just proving the general origin of the observed phenomenon. Noise parameters of the pad-free MOST for the best bias point for different gate width devices were extracted using equivalent circuit method. For the wide gate device the difference between NF_{min} of the pad-free MOST and DUT is smaller, see fig.11, as compared to the narrow gate transistor (device 43, see fig.12) where the pad and gate parasitics significantly degrade noise performance. Extracted *NF(50)* of the pad-free devices evaluate noise performance of the transistor connected in to the 50Ω circuit. Simulated NF_{min} of pads free MOSTs agree well with recently reported NF_{min}=0.37dB at 2GHz (LxW=0.35x300μm^2) where the influence of pads was reduced by means of double sided and shielded-ground pads at the cost of *Gopt* [6]. Extracted Pospieszalski drain temperatures are presented in the captions of the fig.11,12,13. Drain temperatures of the *p* type devices are lower as compared to *n* devices. Nevertheless NF_{min} of pad-free MOST is higher for the *p* type. This means that in *p* devices, contrary to *n* MOSFETs, the contribution of the channel noise to the noise performance of the transistor is less and that the gate resistance thermal noise becomes the dominant. Channel thermal noise in *n* devices due to higher mobility and thus electron heating controls the noise performance of the device.

SUMMARY

The pad parasitic elements significantly affect the microwave noise performance of the submicron gate length MOSFETs, especially for the scaled down gate width devices. The observed resonant maximum in noise and kinks in *s*-parameters at lower drain currents, we think, are associated with influence of the gate parasitic self and mutual inductance. For *p* type, contrary to *n* MOSFETs, the contribution of the channel noise to the NF_{min} is less while NF_{min} is

controlled by the gate resistance thermal noise. In *n* MOSFETs the channel thermal noise due to higher mobility and thus carrier heating controls the noise performance of the device.

References

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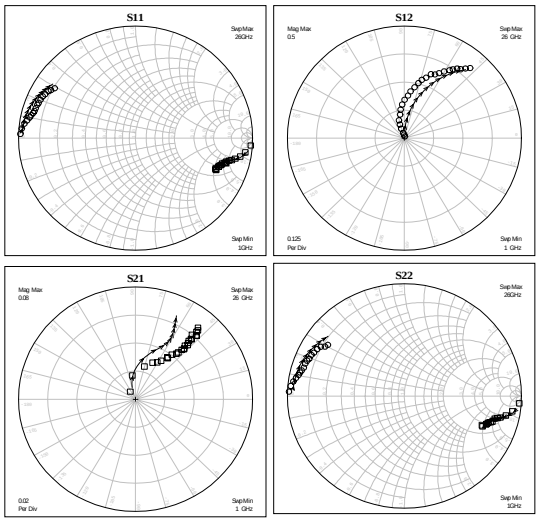

Fig.1. Measured and simulated s-parameters of „open" and „short" dummy patterns.

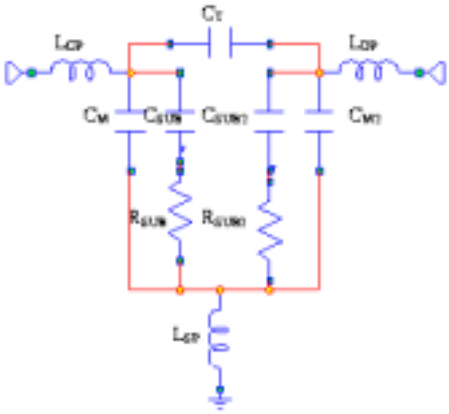

Fig.2. Equivalent circuit model of an „open" dummy pattern.

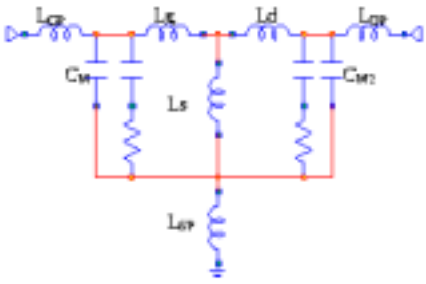

Fig.3. Equivalent circuit model of an „short" dummy structure.

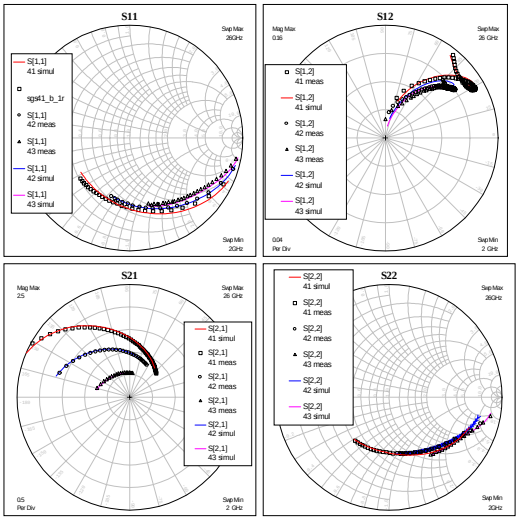

Fig.4. Measured and modeled *s*-parameters of the DUTs. Squares are device 41, open circles are device 42 and triangles correspond to device 43.

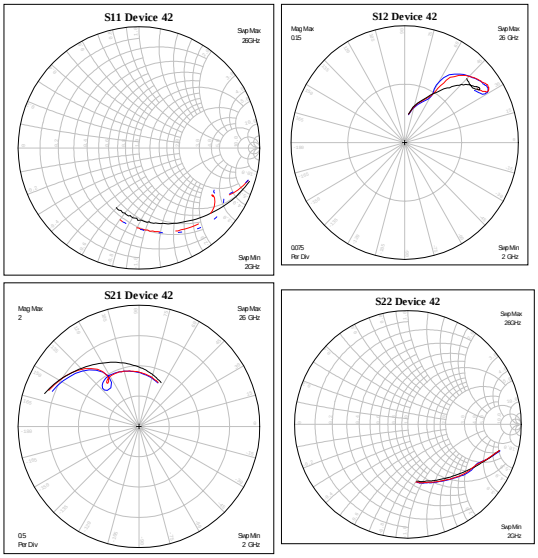

Fig.5. An evolution of measured s-parameters with drain current, (blue line is I_D=8 mA, red line I_D=9.9 mA and black line I_D=11 mA. Device 42).

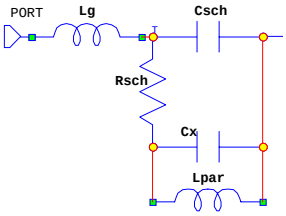

Fig.6. Gate parasitics model. *Lg* is the MOST gate inductance, L_{par} and C_{sch} are the parasitic ind., and capacitance.

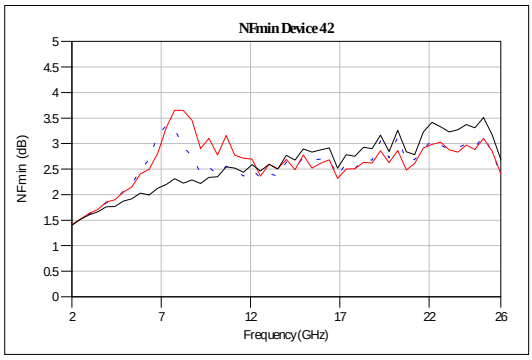

Fig.7. Measured NF_{min} versus frequency, blue line is I_D=8 mA, red line I_D=9.9 mA and black line I_D=11 mA. Device 42.

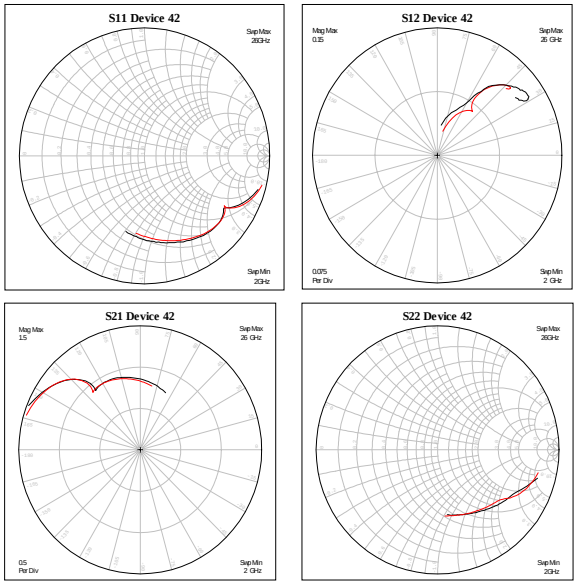

Fig.8. Measured (black line) and simulated (red line) *s*-parameters. I_D=6.3 mA , device 42.

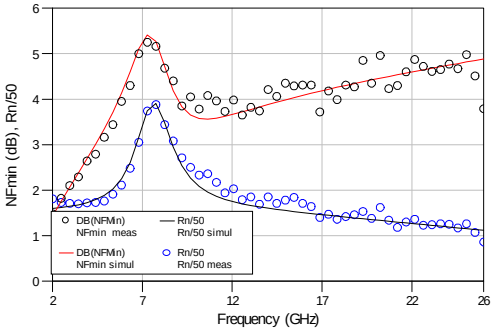

Fig.9. Measured (circles) and simulated (lines) NF_{min} and normalized *Rn* for the device 42 at I_D=6.3 mA.

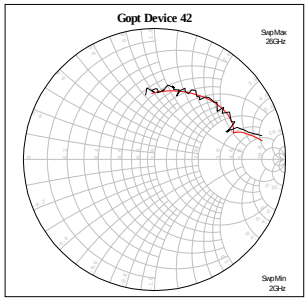

Fig.10. Measured (black line) and simulated (red line) *Gopt* versus frequency I_D=6.3 mA, device 42.

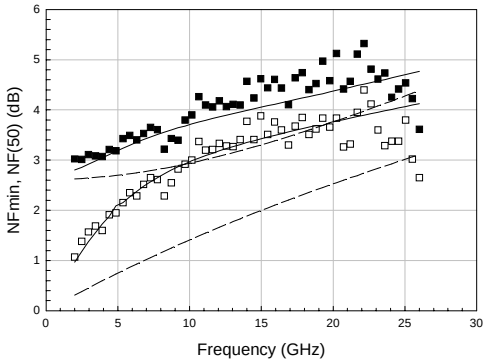

Fig.11. Measured NF_{min}, *NF(50)* (open and solid boxes) and simulated (solid lines). I_D=9.8 mA, device 41. Pads free device is dashed line. T_D= 4350K

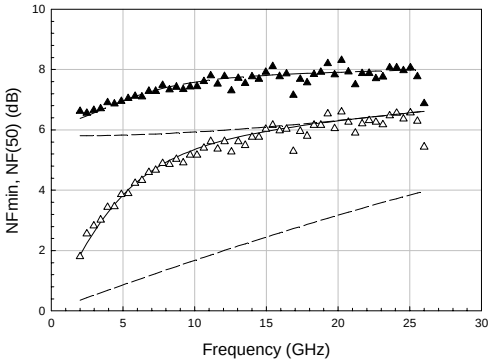

Fig.12. Measured NF_{min}, *NF(50)* (open and solid triangles) and simulated (solid lines). I_D=2.9 mA, device 43. Pads free device is dashed line. T_D= 4495K.

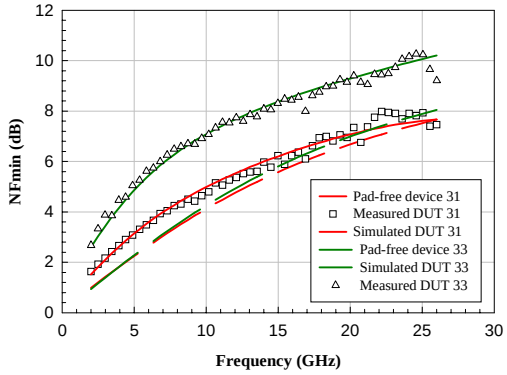

Fig.13. Measured and simulated NF_{min}. I_D=2.9 mA, devices 31, 33. Optimum bias point. T_D= 2050K (31), T_D=1784K (33).