Silicon Micromachined Packages for RF MEMS Switches

Alexandros Margomenos, Dimitrios Peroulis, Katherine J. Herrick, and Linda P. B. Katehi
Radiation Laboratory, Department of Electrical Engineering and Computer Science,
University of Michigan, Ann Arbor, Michigan, 48109-2122, USA.
amargome@engin.umich.edu, katehi@engin.umich.edu

Abstract— **MEMS technology has major applications in developing smaller, faster and less energy consuming devices provided that reliability of packaging/interconnect technology is sufficiently addressed. This paper presents a low cost, on-wafer, silicon micromachined packaging scheme for RF MEMS switches having excellent electrical performance in K-band. In particular, the package demonstrates an insertion loss of 0.1dB and a return loss of 32dB at 20 GHz. The package is fabricated in parallel with the MEMS switch on the same wafer and therefore requires no lossy solder bumps or bond wires to achieve signal propagation.**

Keywords— **micromachining, packaging, RF MEMS switch**

I. Introduction

INTEGRATED circuit packaging and its testing has evolved over the past years due to the maturity of the IC industry, the availability of a highly advanced infrastructure, and the wide applications of the integrated circuits. The goal for IC packaging is to provide an electrical interface to active chips in the system, supply signal power and ground interconnections, allow heat dissipation, and isolate the chips from the environment. Although fabrication techniques can be carried over from IC to MEMS, the requirements of MEMS packaging are different from those of IC packaging since it is application specific and different designs are needed for different circuits. This lack of standardization leads to excessive cost for the final product [1]. Millimeter wave systems for commercial, scientific or military applications are rapidly emerging requiring development of high frequency packaging technologies. For high-density, high frequency (5-100 GHz) packages the performance requirements are very stringent, since poor design and fabrication can lead to increased cavity resonances and cross-talk between neighboring circuits [2]. Many materials can be utilized for packaging including plastic and alumina which offer low cost. Both, however, suffer from poor electrical performance at frequencies beyond 10 GHz. Silicon on the other hand has been extensively used and studied in the electronics industry [3]. Its electrical properties have enabled the semiconductor industry to use it as the primary dielectric material in developing ICs while the mechanical properties of Si have been utilized to develop high performance MEMS structures. These two properties in addition to the thermal characteristics of Si make it an appealing candidate for packaging high frequency circuits.

A low actuation voltage RF MEMS switch has been developed [4] and tested recently to demonstrate actuation voltages as low as 6 Volts with an on-to-off capacitance ratio of 48. Power handling measurements show no ”self-biasing” or failure for power levels up to 6.6 W while, RF measurements demonstrate an isolation of -26 dB at 40 GHz, which can be tuned by appropriately adding inductive beams [5] . The operation of the RF MEMS switch requires DC as well as RF interconnects which carry the DC voltage and RF current from the probe pads to the device. In the proposed architecture the DC and RF pads are printed on the opposite side of the Si wafer that carries the switch (Fig.1) and are then transitioned via appropriate through-wafer transitions designed to operate well both for DC and RF signals [6]. Specifically for the RF transition a 50 Ω FGC line (50-80-50 μm) expands to a much wider 50 Ω FGC line (90-220-90 μm) in order to allow for the anisotropic etching of the vias. The transition has been designed using a method of moments code [7] and optimized for low loss in K-band. A schematic of the transition is presented in Fig.2a.

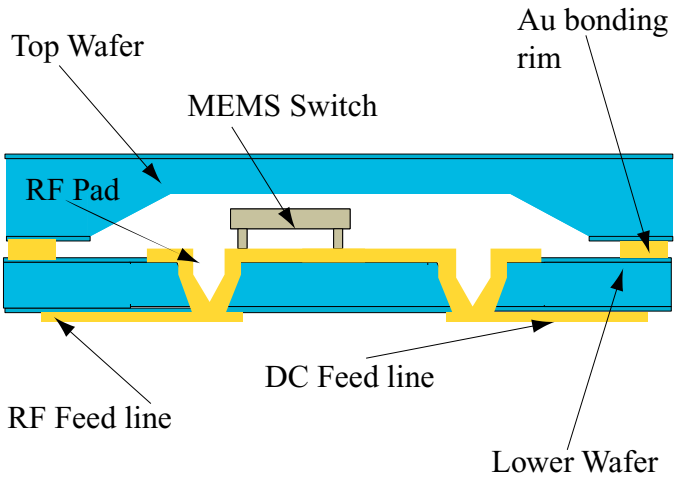
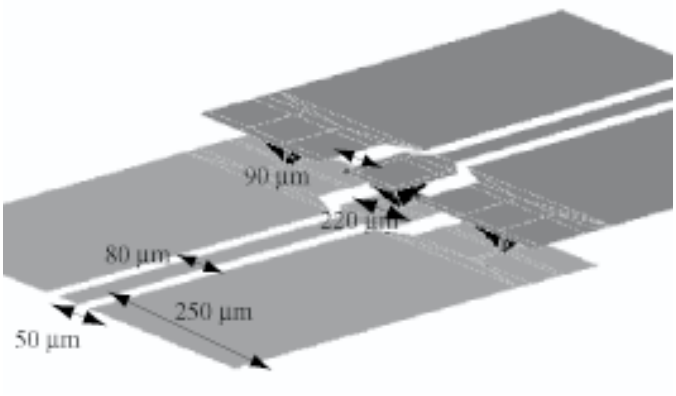


Fig. 1. Schematic of packaged RF switch with DC and RF via transitions.

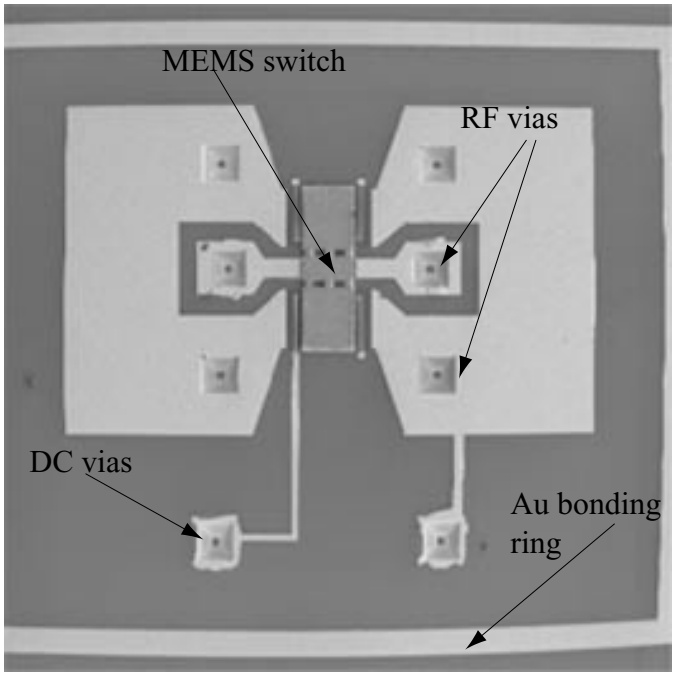
II. Fabrication Process

The fabrication process involves the combination of surface and bulk micromachining. Two 100 μm thick high-resistivity double-side polished silicon wafers with 8700 Å SiO_2 on both sides were used. On the lower wafer:(a) 500/9500 Å of Cr/Au are deposited using lift-off process; (b) SiO_2 is patterned on the top side of the wafer using infrared (IR) alignment and etched fully in buffered hydrofluoric acid (BHF) at a rate of 1000 Å/min ; (c) the oxide-patterned vias are etched in potassium hydroxide (KOH) at an etch rate of 30 Å/hour; (d) using a modified lift-off technique, simultaneous metallization of surface patterns and vias can be achieved. Along with the circuit metal a square rim was patterned around each circuit in order to be used for thermocompression bonding.

The second step was the fabrication of the MEMS switch. The original fabrication process presented in [8] was appropriately modified for compatibility with the via process. On the aforementioned wafer: (a) 2000 Å of plasma enhanced chemical vapor deposition (PECVD) silicon nitride is patterned over the location of switch actuation; (b) a sacrificial layer of 3μm thick polyimide DuPont PI2545 is spun cast, soft baked, and patterned for anchor points; (c) 2 μm of Ni is electroplated to define the switch structure; (d) 4 μm of Ni are selectively electroplated on the switch actuation pads; (e) sacrificial etching of the polyimide layer and supercritical CO_2 drying and release of the switch structure are performed. The outcome of the process is shown in Fig.2b.



(a)



(b)

Fig. 2. (a) Schematic of vertical transition through 100 μm Silicon wafer. (b) SEM of fabricated transition and MEMS switch on 100 μm silicon wafer.

A 100 μm thick Si wafer was used to create the packaging cavity on the top wafer. A lift-off process is used for the metallization of Cr/Au (500/9500 Å) to fabricate a square metallic rim on the lower side of the wafer. SiO_2 is patterned on both sides of the wafer using infrared (IR) alignment to define cavities and probe windows for the final alignment prior to bonding. The SiO_2 is etched partially or fully in buffered hydrofluoric acid (BHF) at a rate of 1000 Å/min. The final step is to anisotropically etch the oxide-patterned cav-

ities and probe windows in potassium hydroxide (KOH) at an etch rate of 30 Å/hour.

Thermocompression bonding of the two wafers is achieved using an Electronic Visions EV 501 Manual Wafer Bonder. The samples are aligned together using the probe windows and fabricated alignment marks. Once aligned the wafers are clamped together in the bond fixture and are heated to 350 degrees Celsius. 200 N of force is applied for 30 minutes on the samples in order to achieve proper adhesion.

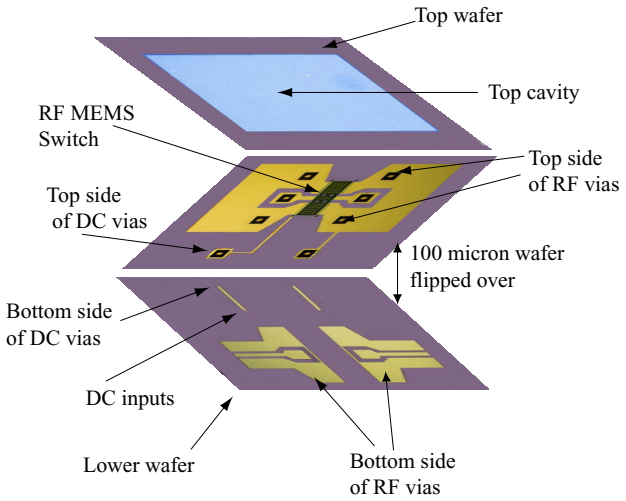


Fig. 3. Photograph of fabricated transition, MEMS switch and packaging cavity.

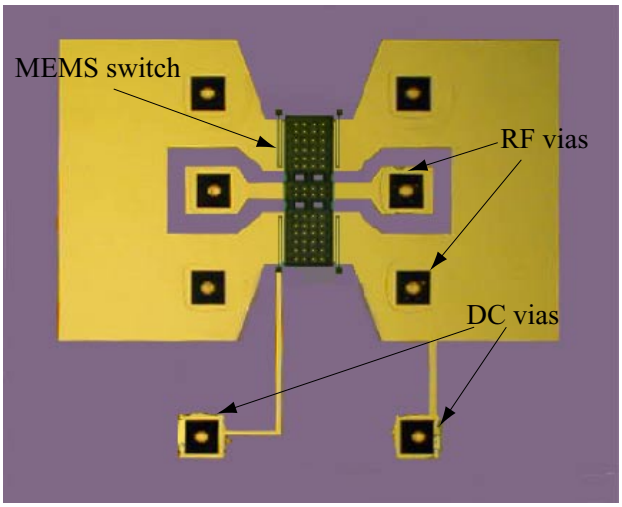


Fig. 4. Photograph of MEMS switch wafer.

III. Measured Results

The packaged switch is presented in Fig.3 where both wafers are shown. In Fig.4 the MEMS switch wafer is presented. The DC vias are connected to the FGC ground plane and to the switch anchor points, while the distance between the RF vias and the switch is 200 μm. In Fig.5 the measured response of the vertical transition is displayed. For the measurements, a HP 8510C vector network analyzer is utilized on an Alessi probe station with 150 μm pitch GGB picoprobes. Through-Reflect-Line (TRL) calibration is performed using on wafer calibration standards fabricated in conjunction with the circuits to be tested. Multical, developed by NIST, is used to implement the TRL calibration [9]. After deembeding the loss of the FGC feeding line the transition demonstrates a 0.1 dB insertion loss, a 32 dB return loss at 20 GHz and a 55% bandwidth. Thus, the loss due to each transition is approximately 0.05dB. One hundred circuits were fabricated with 94% yield and tested with very similar and consistent results.

The RF transition presented is a modification of the silicon micromachined vertical interconnect presented in [6]. These transitions were designed to operate at W-band with an insertion loss of 0.55 dB from which 0.2 dB is attributed to radiation losses and 0.35 dB to ohmic losses. The original interconnect utilized resonant stubs to tune the operating frequency at 94 GHz and thus, it had an inherently narrow bandwidth. The design shown in this study is a scaled model of the aforementioned transition scaled at K-band and therefore it shares a narrow bandwidth as well. Some broadband transitions have also been designed and fabricated and results are going to be presented at the conference.

The subsequent step was to fabricate the MEMS switch on the same wafer (Fig.4). The measured response of this system is presented in Fig.6, where both the up state and down state measurements are included. When the switch is in the up position the response is similar to the one illustrated in Fig.5. The capacitance of the switch at that position is 38 fF and therefore has some minor effects on the response of the circuit. Moreover the loss due to individual MEMS RF switches is in the order of 0.16 dB at 40 GHz [4] and henceforth the insertion loss of the total circuit is increased. The down state capacitance of the switch can be extracted from the S-parameters to be 1.6 pF and the switch demonstrates an isolation of approximately -22 dB at 40 GHz. The resonance occur-

ring around 29 GHz is due to the RF transition, an optimum design of which can increase the bandwidth of operation and remove any unwanted resonances. Comparing the two measurements we can conclude that the operation frequency band for the packaged RF MEMS switch is between 11 and 24 GHz, offering an insertion loss of 0.15 dB (switch loss included) and an isolation of -16 dB at 24 GHz.

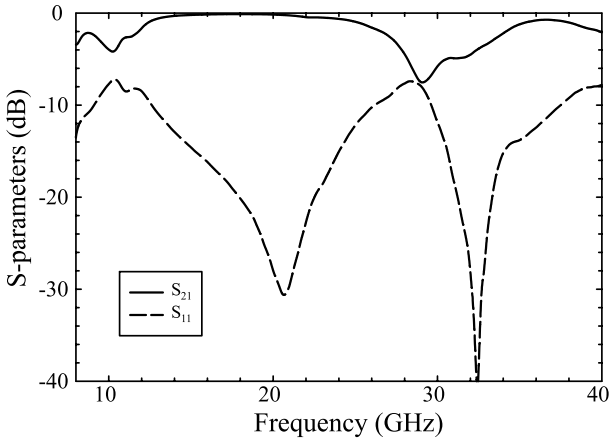


Fig. 5. Measured response of RF transition.

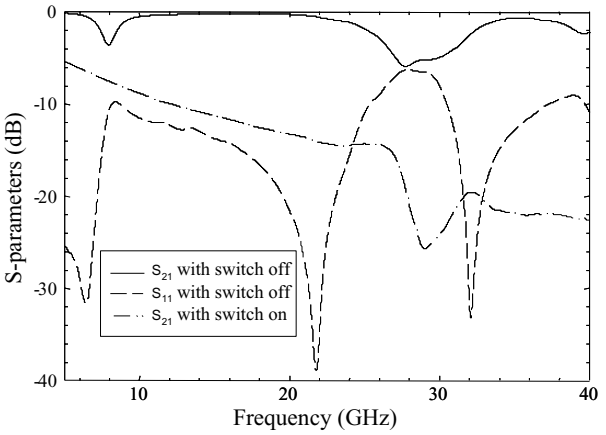


Fig. 6. Measured response of packaged RF switch in on and off position.

IV. Conclusions

Packaging of high frequency MEMS devices is challenging since achieving signal distribution and environmental protection requires careful design and fabrication. A novel on-wafer packaging scheme has been suggested providing promising results for further investigation. Particularly the packaging scheme demonstrates an insertion loss of 0.1 dB and a return loss of 32 dB at 20 GHz. The fabrication process for the package (vertical transition, RF MEMS switch and thermocompression bonding) has been tested providing functional MEMS switches with high yield.

V. Acknowledgements

This work was supported by NSF.

References

[1] R. Ramesham and R. Ghaffarian, "Challenges in Interconnection and Packaging of Micromechanical Systems (MEMS)," in *2000 Electronic Components and Technology Conference*, May 2000, pp. 666–675.

[2] A. Margomenos, S. Valas, M.I. Herman, and L.P.B. Katehi, "Isolation in Three-Dimensional Integrated Circuits," in *2000 IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, June 2000, pp. 1875–1878.

[3] R. M. Henderson, *Silicon-Based Micromachined Packaging Techniques for High Frequency Applications*, Ph.D. thesis, University of Michigan, Ann Arbor, MI, 1999.

[4] S.P. Pacheco, L.P.B. Katehi, and C.T.C. Nguyen, "Design of Low Actuation Voltage RF MEMS Switch," in *2000 IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, June 2000, pp. 167–170.

[5] D. Peroulis, S.P. Pacheco, K. Sarabandi, and L.P.B. Katehi, "MEMS Devices for High Isolation Switching and Tunable Filtering," in *2000 IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, June 2000, pp. 1217–1220.

[6] K.J. Herrick, *W-Band Three-Dimensional Integrated Circuits Utilizing Silicon Micromachining*, Ph.D. thesis, The University of Michigan, Ann Arbor, MI, 2000.

[7] Zeland Software, Inc., Fremont, CA, *IE3D User's Manual, Release 8*, 2001.

[8] D. Peroulis, S.P. Pacheco, K. Sarabandi, and L.P.B. Katehi, "Alleviating the Adverse Effects of Residual Stresses in RF MEMS switches," in *2001 European Microwave Conference*, September 2001.

[9] R.B. Marks and D.F. Williams, "Program MultiCal, rev. 1.00," August 1995.