A 2GHz Delta-Sigma Modulator implemented in InP HBT technology

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ABSTRACT

A first-order Delta-Sigma (ΔΣ) modulator has been fabricated using a 70GHz (f_T) AlInAs/GaInAs-InP HBT technology. At a sampling rate of 2GHz, it converts a 50MHz signal with a maximum signal-to-noise ratio (SNRmax) of 19dB and a dynamic range (DR) of 25dB, equivalent to 3.9DRbits. With a 10MHz signal, 36.5dB DR (5.8DRbits) and 30.8dB SNRmax are achieved. The modulator has been designed in a fully differential architecture, and dissipates 330mW from a -5V power supply. This paper presents the performance of a first-order, continuous-time, low-pass ΔΣ modulator. To date only a few results have been reported for first-order ΔΣ modulator implemented in a III-V technology. A first-order architecture represents a fundamental first step in the design of higher order modulator offering better performance.

1. INTRODUCTION

High-speed analog-to-digital converters (ADC) are becoming increasingly popular in applications requiring signal processing of wide-band signals. The benefits of using digital signal processing (DSP) over analog processing techniques can be only realised once the wideband signal has been digitised, hence the need for high-speed ADCs. DSP techniques lead to improvements in system cost, system reproducibility and sensitivity to temperature and environmental variations. System flexibility can also benefit as DSP blocks can be reprogrammed to provide new functionality.

The ΔΣ modulation architecture is known for its ability to perform precise analog-to-digital conversion [1, 2]. This technique combines oversampling and noise-shaping to improve ADC resolution: the noise from the quantizer is shaped away from the signal band prior to being filtered in the following stage by a process called decimation.

InP-based HBT technology is used to implement this circuit. The InP process offers many advantages over GaAs process including reduction in the power consumption, improvement in the speed of operation, lower 1/f noise, lower phase-noise, higher current gain at low current densities and higher thermal conductivity.

The ΔΣ modulation technique when implemented in an InP HBT technology allows the digital conversion of a wideband analog signal to be done at high-speed and with high accuracy. The design of our first-order low-pass continuous-time ΔΣ modulator is described in section 2 and the measured results detailed in the section 3.

2. CIRCUIT DESIGN

The aim of this work is to investigate the development of a high frequency ΔΣ modulator to digitise IF frequencies signals in a telecommunications receiver. We have chosen to use a continuous-time implementation [3]. A first-order topology offers a 9dB SNR improvement for each doubling of the sampling frequency. Second and higher order modulators give better performance [4, 5] but they are more complex to design and require sharp filtering in the decimation stage. A first-order implementation was undertaken to prove the concept and establish the fundamental design considerations.

The architecture of the system is illustrated in figure 1. A fully differential configuration has been chosen for higher linearity and improved DR. The first-order continuous-time ΔΣ modulator includes a transconductance cell converting a differential voltage to a differential current signal, an integrator to filter the noise away from the amplified signal, a one-bit ADC to quantize the signal and a one-bit digital-to-analog converter (DAC) in the feedback loop.

The linearity of the transconductance cell (figure 2) is critical for the overall performance of the system, as it is located at the input to the modulator and outside of the feedback loop. For this reason, two transconductance cells are used together to reduce the distortion to a minimum while maintaining a large flat gain versus frequency performance.

The integrator (figure 3) provides noise shaping as it accumulates the large quantization error from the one-bit ADC. It is formed from a three stage amplifier with two integrating capacitors connected between its input and output.

The one-bit ADC (figure 4) is a classic comparator using a master-slave architecture and has a significant impact on the final resolution of the ΔΣ modulator. Hysteresis and metastability arising from this component are the limiting factors when the input voltage is decreased or the sampling frequency is increased.
Finally the DAC in the feedback loop is a one-bit current steered differential pair. Two bias current sources are connected to the feedback node to sink the quiescent current of the transconductance cell and DAC.

3. MEASURED RESULTS

The fabricated ΔΣ modulator is shown in Figure 5. The circuit includes 88 transistors in a 1.0 x 1.7 mm^2 die size. It operates from a –5V power supply and dissipates 330mW.
The measurements were completed on wafer using a high frequency Cascade probe card. Observations of the pseudo-random digital output were captured on a 20GSp/s Agilent digital oscilloscope. Figure 6 shows an eye diagram of a 50MHz input signal sampled at 2GHz. Two Anritsu synthesizers are used for the clock and the ΔΣ modulator inputs. 2GHz was found to be the maximum rate at which the ΔΣ modulator could be clocked. Above this frequency, the rise and fall time necessary for the ΔΣ modulator to switch correctly from one level to the other start to exceed the sampling period. This limitation is due to the metastability of the one-bit ADC and can be improved by adding a third stage of latch buffering after the master-slave ADC.
Figure 7 shows two output spectrums sampled with a 500MHz and a 2GHz clock frequency. The performance was measured with a HP spectrum analyser. The noise at the lower frequency is clearly shaped away to higher frequency and the SNR of the 50MHz input signal is improved with increasing clock frequency. We also notice harmonic signals at multiples of the signal frequency. These tones are visible at large input amplitudes, (in this case 0dBm). These spurious are likely to be limit cycle tones directly related to the quantization error. First order modulators are known to be more susceptible to limit cycle tones than higher-order topologies. These tones arise because the quantisation error is correlated with the input signal. It is important to take this into account, as linear models of ΔΣ modulators do not predict limit cycle tones. They assume the quantization error to be uncorrelated white noise. A solution is to add dither to the input signal to force it to be “busy” but with an associated reduction in SNR [6].
To evaluate the performances of the ΔΣ modulator, the SNR (including distortion tones) has been measured with a range of input power values at different clock frequencies. The results are plotted in figure 8. With a 50MHz signal, the SNRmax are 7.6dB, 13.4dB and 19dB for 500MHz, 1GHz and 2GHz sampling frequencies respectively. Measurements were also made for a 10MHz signal. For the same sampling frequencies, SNRmax of 21.9dB, 26.4dB, 30.8dB are obtained respectively. The ideal improvement of the SNR at a specific input magnitude for each doubling clock frequency is about 9dB for a first-order ΔΣ modulator. In practice, we obtain up to 8dB improvement.
The DR corresponds to the input amplitude range for which the SNR is positive in the linear area. For the 50MHz bandwidth signal, its value is about 9, 19 and 25dB for 500MHz, 1GHz and 2GHz clock frequencies respectively. This corresponds to 1.2, 2.9 and 3.9DRbits. Better dynamic ranges are obtained for the narrower 10MHz signal bandwidth as the oversampling ratio is increased. For the same sampling frequencies, the DR is approximately 28dB, 32.5dB, and 36.5dB respectively, representing 4.3, 5.1 and 5.8DRbits.

4. CONCLUSION

A first-order, continuous-time ΔΣ modulator has been successfully implemented in an AlInAs/GaInAs-InP HBT technology. At a sampling rate of 2GHz, it converts a 50MHz signal bandwidth with a SNRmax of 19dB and a DR of 25dB, equivalent to 3.9DRbits. With a 10MHz signal, 36.5dB DR (5.8DRbits) and 30.8dB SNRmax are achieved at the same sampling frequency. The circuit presented in this paper indicates the potential for ΔΣ modulators to provide high-speed digitisation of IF frequencies in a telecommunications receiver. This design represents the first stage of our development of high-speed high-order ΔΣ modulators.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

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7. FIGURES

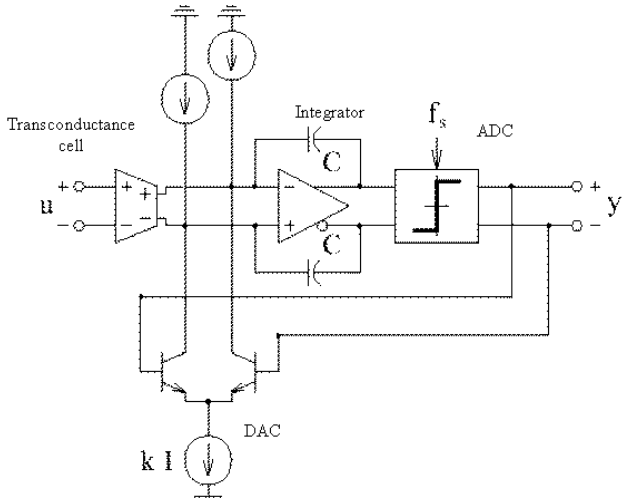


Figure 1. Simplified diagram of the first-order ΔΣ modulator.

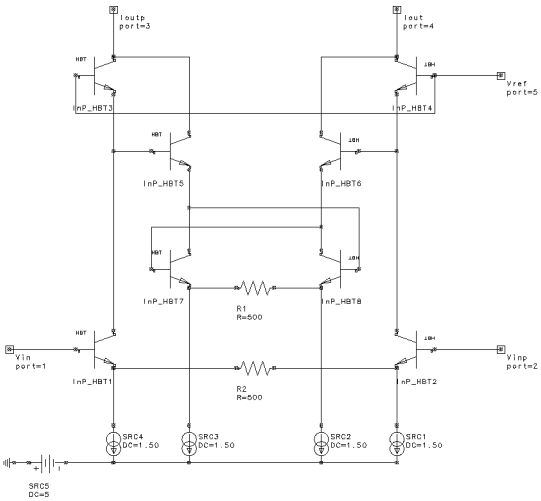


Figure 2. Schematic diagram of the transconductance cell.

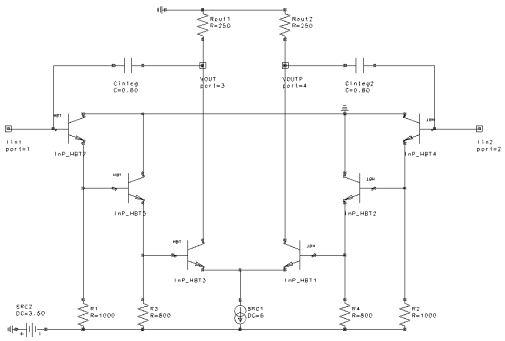


Figure 3. Schematic diagram of the integrator.

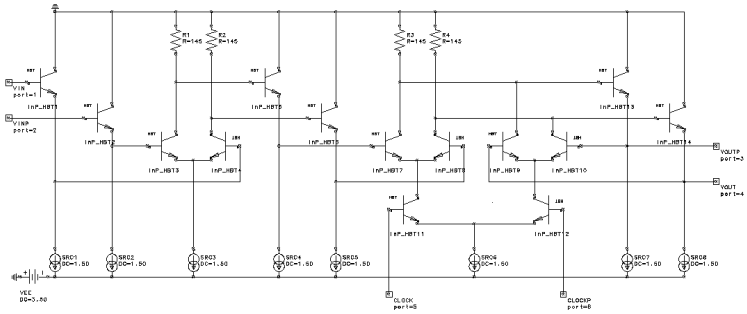


Figure 4. Schematic diagram of the ADC (with master stage only).

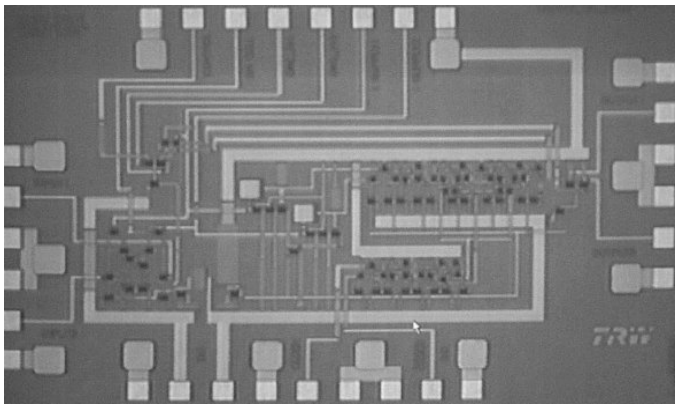


Figure 5. Die photograph of the first-order ΔΣ modulator.

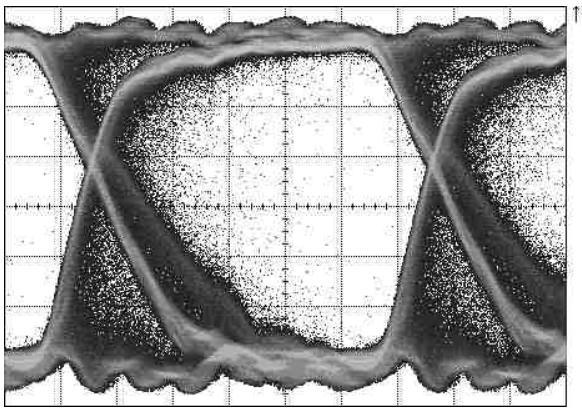
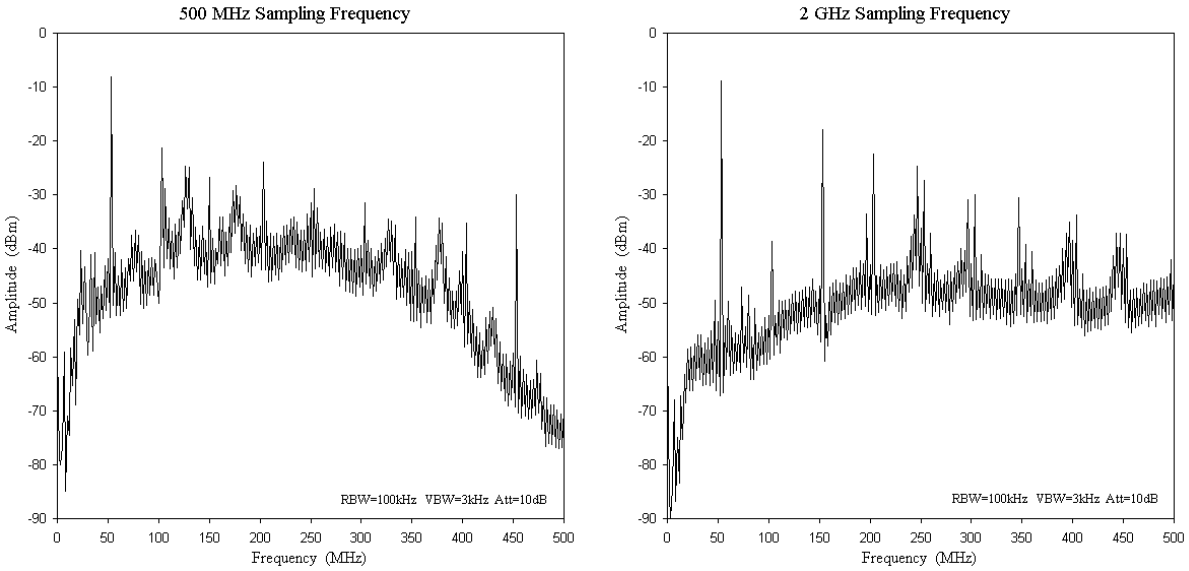
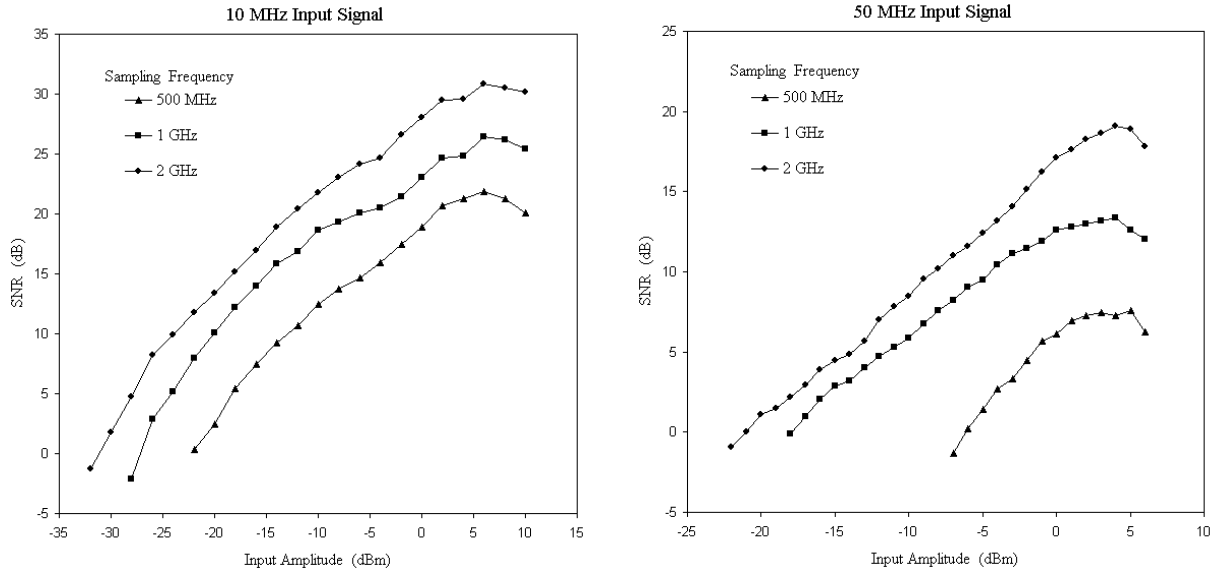


Figure 6. Eye diagram of a 50MHz signal sampled at 2GHz.



(a) (b)

Figure 7. Frequency spectra measured from a 50MHz and 0dBm input signal at clock frequencies of (a) 500MHz and (b) 2GHz.



(a) (b)

Figure 8. SNR obtained from a (a) 10MHz and (b) 50MHz signal with three clock frequencies, 500MHz 1GHz and 2GHz.