A simple condition for maximum bandwidth of a chip packaged in an mm-wave waveguide

Adam K. Jastrzebski

Department of Electronics, University of Kent, Canterbury, Kent, CT2 7NT, UK
Phone +44 1227 823704; Fax +44 1227 456084; E-mail A.K.Jastrzebski@ukc.ac.uk

Abstract- *Waveguides can be used as both packaging cases and interconnection media between chips. No bond wires are needed in this packaging technique and, consequently, it can be used in millimetre wave circuits and systems. However, a chip inserted in a waveguide introduces additional unwanted propagation modes and reduces an effective bandwidth of the structure. A simple condition for an optimum placement of the chip to maximise the bandwidth is derived and confirmed by a rigorous 3-D electromagnetic simulation of WR6 and WR10 waveguide packages for typical GaAs and InP chip dimensions.*

INTRODUCTION

Complex millimetre wave systems are difficult to construct due to packaging problems. Various monolithic active chips need to be interconnected with each other, but standard techniques, such as bond wires cannot be used due to large unknown parasitics. One of the possible solutions, still under development [1], is to use waveguides both for packaging and as interconnection media, with electromagnetic coupling between the chips and the waveguide. The simplest approach is to place the chip with suitable input and output slotline tapers in the E-plane of the waveguide (see Fig. 1). However, the effect of high permittivity (12.9 for GaAs) of a semiconductor chip on propagation modes in a waveguide needs to be investigated. Traditionally, finline structures consisting of a dielectric with a slotline placed in the E-plane were used to reduce the lower cut-off frequency of the fundamental mode, enabling usage of relatively small dimension waveguides at low frequencies. Unfortunately, the cut-off frequencies of the higher order modes are also reduced. When a waveguide is used as both interconnection medium and a package, then a useful bandwidth of the whole system is between the cut-off frequency of the fundamental mode of the empty waveguide and the first higher order mode of the waveguide with the chip. The electric loading from the semiconductor substrate of a chip and the slotline circuitry on it can dramatically reduce the cut-off frequencies of higher order modes and consequently cause severe reduction in a useful system bandwidth. These effects have been already investigated in [2]. For example for WR6 waveguide, when a finline with a relatively thick substrate of 200μm is used, the cut-off frequency of the first higher order mode is only 112 GHz, which is below the lower frequency of the practical bandwidth of a hollow WR6 waveguide. Waveguide packaging cannot be used in this case, as there is no useful bandwidth in the system. One way to increase the bandwidth is to use a very thin chip substrate. However, thinning GaAs or InP semiconductor substrates is not only quite expensive, but also produces very brittle chips that are difficult to handle. An alternative solution was proposed in [3], in which the slotline was mounted at an offset in a plane with zero electric field for TE_{20} mode, rather than in the centre of the waveguide. It was shown that the frequency of the first higher order mode of the WR6 waveguide with a 200μm chip has increased by 14 GHz to 126 GHz, representing a substantial improvement. In this paper we use transverse resonance analysis to derive a simple implicit condition for an optimum offset of the chip. We compare the results obtained by the solution of this condition with those obtained from rigorous 3-D electromagnetic simulations of WR6 and WR10 waveguide packages for typical GaAs and InP chip dimensions, showing excellent agreement.

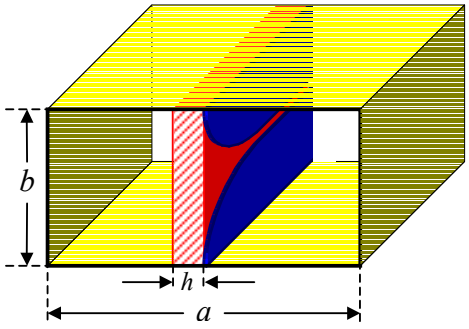


Figure 1. Waveguide with a chip in the E-plane (only the taper section of the chip is shown).

WR6: a = 1.651 mm, b = 0.826 mm, practical bandwidth 114 – 173 GHz.
WR10: a = 2.54 mm, b = 1.27 mm, practical bandwidth 73.8 – 112 GHz.
Chip: permittivity 12.9, thickness h = 100 – 200 μm.

TRANSVERSE RESONANCE ANALYSIS OF AN OFFSET FINLINE

As it was shown in [2] and [3], the cut-off frequency for the TE_{20} mode, f_{c20}, is responsible for the reduction of the useful bandwidth of the waveguide packaging structure in Fig.1. From the transmission line theory, the cut-off frequencies for the dominant mode and the higher order modes with vertical electric fields can be determined for this structure from the transverse resonant condition [3]. Fig. 2 is a cross-sectional view of the finline and its equivalent transverse network is shown in Fig. 3. Points A and D correspond to short-circuits created by waveguide walls. The equivalent network consists of three parallel-strip transmission lines and the capacitance C_f representing the finline gap. For simplicity, the strips can be assumed to have a unit width. Instead of positioning the slotline in the E-plane at the centre of the waveguide, which is the case for the previous applications of finlines, the slotline is placed with an offset δ from the centre. When the electric field corresponding to TE_{20} mode is zero at the offset point B, there is no effect of the slot line metalisation represented by the capacitance C_f and f_{c20} reaches maximum.

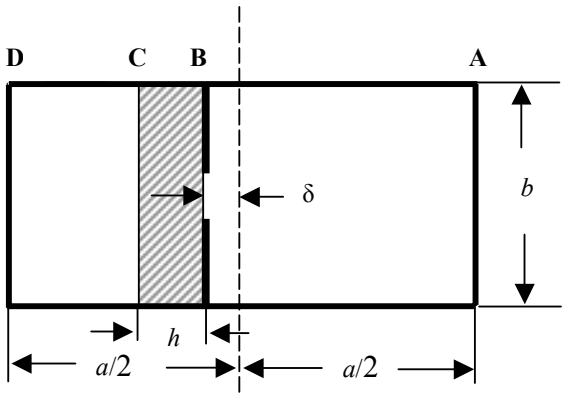


Figure 2. Cross-sectional view of a finline with offset δ

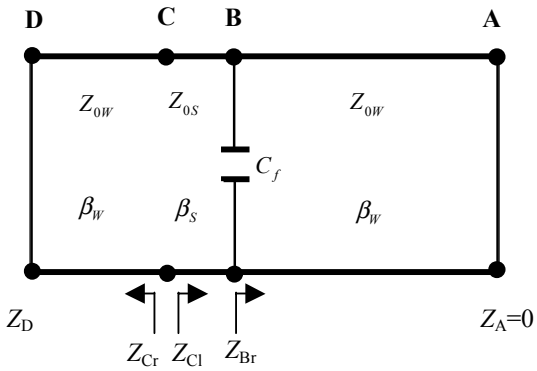


Figure 3. Equivalent transverse network of a finline

For the electric field at point B to be zero, the impedances transformed from A to B and from D to B must be zero. Referring to Fig. 3, the equivalent conditions are:

$$Z_B = jZ_{0W}\tan(\beta_W(\frac{a}{2}+\delta)) = 0 \quad => \quad \beta_W(\frac{a}{2}+\delta) = \pi \tag{1}$$

$$Z_{Cr} = Z_{Cl}^* \quad => \quad jZ_{0S}\tan(\beta_S h) = -jZ_{0W}\tan(\beta_W(\frac{a}{2}-h-\delta)) \tag{2}$$

Where:

$$\beta_W = 2\pi/\lambda_0, \quad \beta_S = \beta_W\sqrt{\varepsilon_{rS}}, \tag{3}$$

$$Z_{0W} = 120\pi b, \quad Z_{0S} = \frac{Z_{0W}}{\sqrt{\varepsilon_{rS}}}, \tag{4}$$

β_W and β_S are the phase constants in the air and substrate regions, respectively; λ_0 is the wavelength in air, ε_{rs} and h represent dielectric constant and thickness of the substrate, respectively; Z_{0W} and Z_{0S} are the characteristic impedances per metre width of a parallel-strip line with separation b between the strips filled with air and the substrate, respectively; and a and b are the broad and narrow dimensions of the waveguide, respectively.

Substituting into (2) from other equations, gives the condition for the chip offset δ, which maximises the bandwidth

$$-\tan\left(\pi\frac{a/2-h-\delta}{a/2+\delta}\right) = \frac{1}{\sqrt{\varepsilon_r}}\tan\left(\pi\frac{h\sqrt{\varepsilon_r}}{a/2+\delta}\right) \tag{5}$$

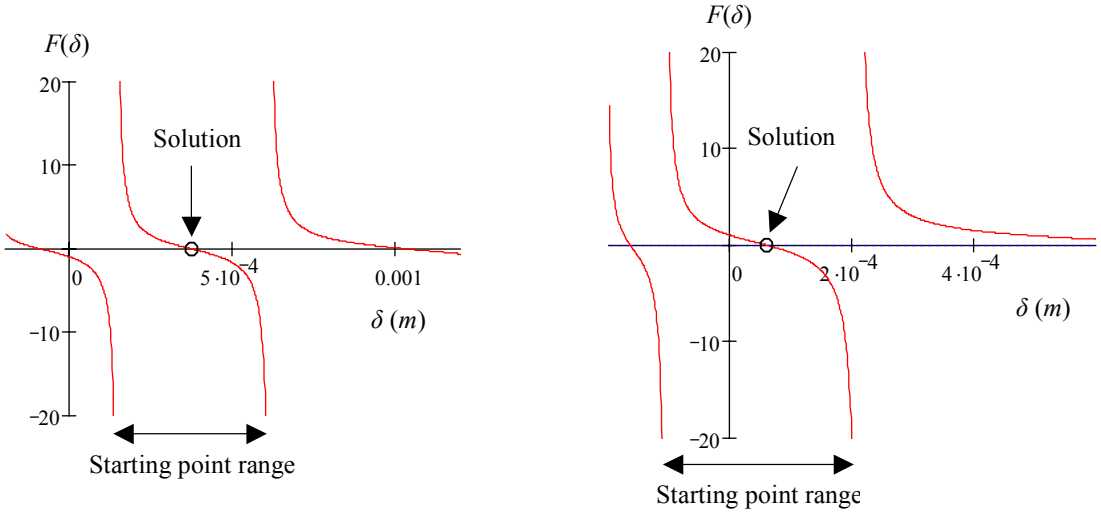
For the known value of δ, the corresponding cut-off frequency for the TE_{20} mode can be calculated from

$$f_{20} = \frac{c}{2(a/2+\delta)} \tag{6}$$

SOLUTION ALGORITHM

Transcendental equation (5) can be solved by an iterative algorithm which finds roots of the function $F(\delta)$ defined by:

$$F(\delta) = \tan\left(\pi \frac{a/2 - h - \delta}{a/2 + \delta}\right) + \frac{1}{\sqrt{\varepsilon_r}} \tan\left(\pi \frac{h\sqrt{\varepsilon_r}}{a/2 + \delta}\right) \tag{7}$$



(a) $h = 0.2$ mm (b) $h = 0.1$ mm

Figure 4. Plots of function $F(\delta)$ for GaAs chip in WR6 waveguide for two values of the chip thickness

Typical plots of $F(\delta)$ are shown in Fig. 4. As it can be seen, this function has multiple roots. Only the solutions fulfilling the following condition make physical sense.

$$0 \le \delta \le \frac{a}{2} - h \tag{8}$$

If a simple iterative root finding algorithm is used, then there is no guarantee that the correct solution is found. Therefore, a good starting point δ_0 is required. The range of acceptable starting points is indicated on the graphs in Fig. 4. An approximate value for δ_0 can obtained by making a simplified assumption that the phase is changing continuously in the transverse resonance analysis. Referring to Figures 2 and 3, this assumption gives the phase change from point D to point B equal approximately to π, i.e.

$$\beta_W (a/2 - h - \delta) + \beta_S h \approx \pi \tag{9}$$

As the same phase change is also between points A and B then using (1), we obtain

$$\delta_0 \approx \frac{h(\sqrt{\varepsilon_r} - 1)}{2} \tag{10}$$

The above starting value has been found to give correct results for the cases considered in this paper. However, if in any doubt regarding the obtained solution, then the conditions (8) and (9) need to be checked.

COMPARISON WITH 3-D ELECTROMAGNETIC SIMULATIONS

The results derived from equations (5) and (6) have been compared with the rigorous 3-dimensional electromagnetic simulation using Agilent HFSS™. The comparison is given in Table 1. The accuracy of the cut-off frequency simulation was 1 GHz. The dependence between the cut-off frequency f_{c20} and the offset δ has a very well defined maximum for substrates that are relatively thick in comparison with the waveguide dimensions (e.g. see Fig. 2 in [3]). Therefore, the accuracy of determining of an optimum offset by simulation is very good in this case. However, when the substrate is relatively thin, then the maximum is quite flat and this gives a large range of offsets for simulation

resolution of 1 GHz. With this in mind, there is an excellent agreement between the theory and the simulation. The results are also in excellent agreement with those obtained by the alternative analytical approach used in [3].

Table 1. Calculated and simulated cut-off frequencies (f_{c20}) of the TE_{20} finline mode in WR6 and WR10 waveguides for different thicknesses (h) of the GaAs chip substrate at an offset (δ) maximising f_{c20}. Bandwidth gain in comparison with zero offset is also shown.

Waveguide	Chip thickness h (μm)	Optimum chip offset δ (μm)		f_{c20} (GHz)		Bandwidth enhancement (GHz)
		Calculated	Simulated	Calculated	Simulated	
WR6	200	364	360	126	126	14
WR6	100	55	45	170	171	5
WR10	200	223	200	100	101	5

CONCLUSIONS

The derived condition (5) enables fast and accurate calculation of the optimum offset of the chip in the waveguide package to maximise the available bandwidth. The corresponding cut-off frequency for the TE_{20} mode can be then simply calculated from (6). Some care needs to be applied when solving the transcendental equation (5) by an iterative algorithm. A suitable choice of a starting point and the conditions verifying the correctness of the solution are proposed. These equations are accurate and far easier to use than electromagnetic simulation.

REFERENCES

1. S.Lucyszyn, S.R.P.Silva, I.D.Robertson, R.J.Collier, A.K.Jastrzebski, I.G.Thayne, S.P.Beaumont: "Terahertz Multi-Chip Module (MCM) Technology for the 21st Century?" IEE Colloquium on Multi-Chip Modules and RFICs, London, May 1998
2. Daiqing Li, Adam Jastrzebski, Richard Collier and Jimmy Yip, "Interaction Between Chip And Its Packaging Waveguide At Millimetre Wave Frequencies", 30 European Microwave Conference, Paris, pp.191-194, October 2000.
3. D.Li, A.Jastrzebski, R.Collier and J.Yip, "Bandwidth enhancement of finline at millimetre-wave frequencies", IEE Electronics Letters, vol. 36, pp 1390-1391, 2000.