25W C-BAND HIGHLY EFFICIENT ON BOARD HYBRID AMPLIFIER

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ABSTRACT - A very high efficient, low distortion C-band power amplifier using a linear and non-linear models of the PHEMT devices has been developed. Single stage amplifier fabricated with 4x18mm gate width PHEMT devices exhibits a power output of 44 dBm at 2dB of gain compression, a linear gain of 11.5dB and an associated PAE from 50% to 52% in the frequency range of 3.6-3.9GHz.

These excellent results are performed by developing an accurate non-linear model of the PHEMT device, the 2.5D electromagnetic simulation of the passive structures and optimizing the output matching network of the amplifier by using a high dielectric substrate with low insertion loss.

I. INTRODUCTION

The power stage of the transmitter amplifier of a satellite equipment requires not only high power added efficiency for optimum dc-power handling, but also high linearity, both requirements are contradictory.

In order to increase linearity a conventional amplifier usually has to be driven with a sufficient input power back-off, whereas high PAE can only be achieved when the amplifier operates in gain compression.

PHEMT devices are becoming a very attractive choice for use in microwave power amplifiers due to specific characteristics such as high gain, linearity and high output power [1] [2].

In recent years, power amplifiers up to 15W have been designed using full MMIC approach to achieve low cost and wide band operation modules [3] [4].

The use of hybrid technology is a right choice for achieving the output power higher than 20W at C-band.

The hybrid technology has the following advantages over the full MMIC approach:

- Higher output power and higher PAE.
- Less losses for the output matching network (increase of 0.5dB on the output power).
- Improved harmonics load.
- Fine tuning of the output stage to compensate for manufacturing dispersion.
- Less GaAs surface and consequently higher manufacturing yield.
- Shorter manufacturing cycle.

In this paper, we present the results of a power amplifier at C-band using PHEMT devices to achieve a power output of 25W.

II. AMPLIFIER DESIGN

The small and large signal device models are used in the design of the power amplifier.

A small cell of 1.2mm periphery is characterized with small-signal S parameters measurements and DC pulse tests. These measurements allow extracting the electrical parameters of linear and non-linear models. General rules of scaling are used in order to obtain the electrical model parameters of power PHEMT devices used in the power amplifier [5] [6].

The amplifier employs four times 18000µm PHEMTs (0.5µm PHEMT from Triquint Semiconductor Texas). To reduce the size of the amplifier, the input and the output matching networks are designed on a high dielectric substrate with low insertion loss. To avoid imbalance operation, each couple of PHEMT is connected by gate and drain stabilizing resistors. To obtain the optimum power performance, a load pull simulation was performed with in-house model using Libra simulator (HP-EEsof). The output network is designed in order to reduce the output section losses and optimize the matching network by a small additional tuning.

From calculated optimum load reflection coefficient and S-parameters at the device level (for achieving the maximum PAE), we determined the source and the load equivalent circuits. Then the matching networks of the power amplifier are optimized by the harmonic balance simulator to achieve the optimum combination of high output power and high PAE [7] [8] [9]. A full wave electromagnetic simulation (Momentum) was performed for passive structures to eliminate the uncertainties caused by the quasi-static models.

The RF and DC decoupling as well as the bias circuits are included in the power amplifier to make it a self-content module without the need of outside circuitry. The linear response of the amplifier is shown in the figure 1.

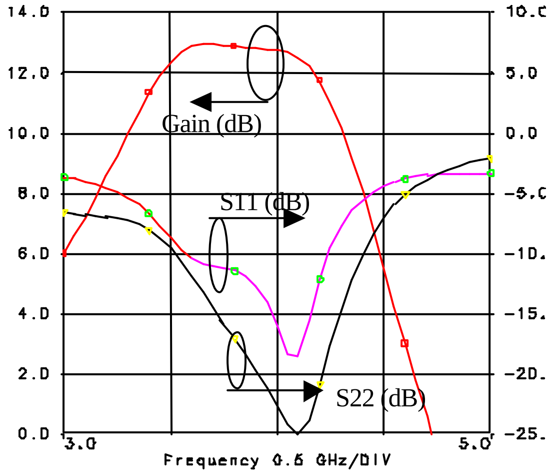

Fig.1: Simulated linear response of the amplifier

The simulated AM/AM response of the power amplifier at Vds=6V is shown in the figure 2. The output power is higher than 44 dBm, with the associated PAE greater than 53% over the frequency range of 3.6 –3.9GHz.

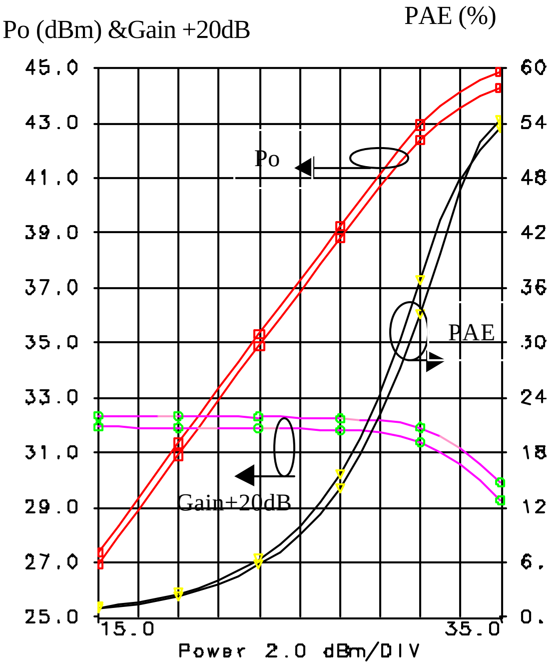

Fig.2: Simulated Po, Gain+20 dB, and PAE of the amplifier (BW=300 MHz)

The simulated load cycle of one of the devices for the input power of 35 dBm (≅ 3 dB of gain compression) is given in the figure 3. The power consumption of each device is corresponding to the area of the curve I-V. The reduced area of the curve for Pin = 35 dBm demonstrates that each device is optimized for the high power added efficiency.

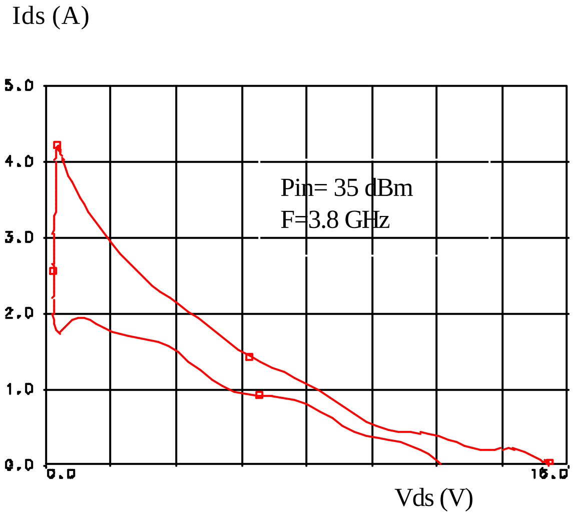

Fig.3: Simulated load cycle of one of the devices

The stability of the amplifier has been intensively studied using different methods. First, the conditions in Rollett's factors have been checked (K>1, B>0) as shown in the figure 4. Then the Nyquist Determined Factor (NDF) analysis has been performed and different odd mode stability elements (gate to gate and drain to drain resistors) have been optimized. The amplifier is stable because the network does not contain any pole in the right half plan [10] [11].

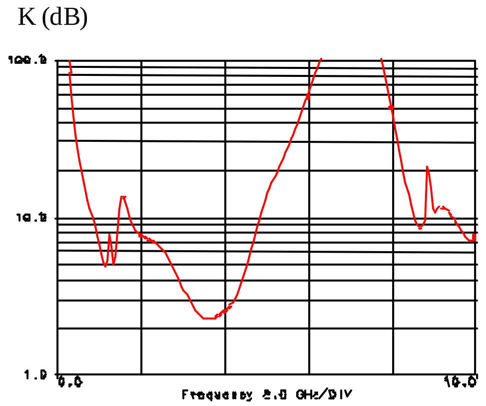

Fig.4: K-factor of the amplifier

Finally the stability of the amplifier during the switch-on has been analyzed by the time domain method. The PHEMT devices operating at class A\B might present the parametric oscillations [12]. These oscillations can be generated during the switching phase of the power amplifier. In order to detect these oscillations, a time domain analysis of the amplifier is required.

The microwave Spice simulator has been used to analyze the time domain response of the device under a step DC voltage. The drain current of PHEMT devices reach the steady state in less than 0.5µs (see figure 5).

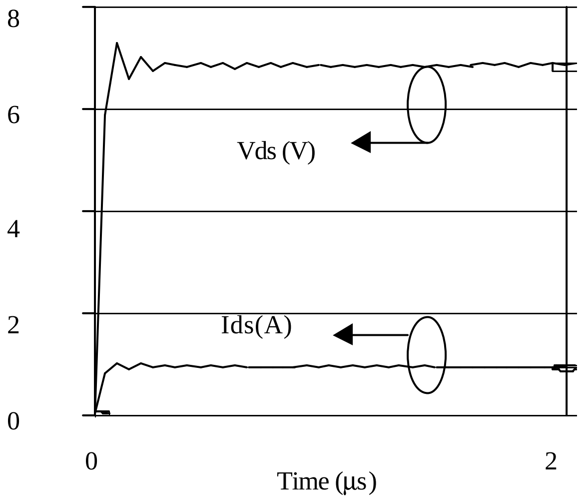

Fig.5: Time domain response of the amplifier
(Simulation for each 18mm device)

Mastering the non-linear model allows simulating the instantaneous non-linear gate forward current and gate-drain breakdown voltage to check that the power module is designed in a safe operating area. Because reliability is of extremely high importance for space application, this methodology is a major advantage over the more classical approach based on life test data only.

Figure 6 presents the instantaneous gate-drain voltage at F=3.8 GHz and for the input power of 35 dBm (≅3 dB gain compression).

The minimum value of the gate-drain voltage is lower than –17V which is far away from the gate-drain breakdown voltage.

The simulations can be validated by the RF burn-in tests.

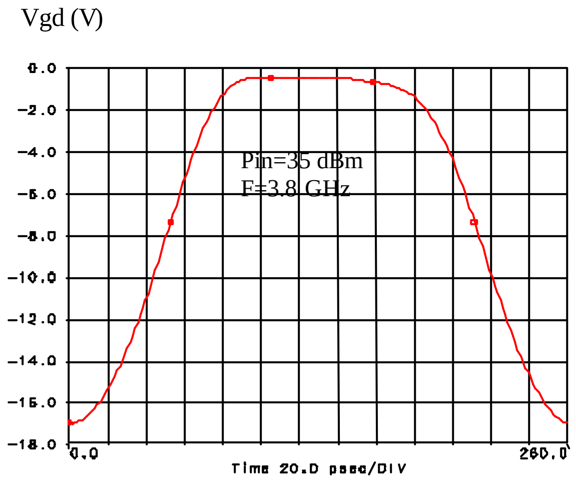

Fig.6: Instantaneous Gate-Drain Voltage of the device
(Simulation for each 18mm device)

A thermal model has been realized by taking into account the topology of the PHEMT devices, and the packaging of the power amplifier. The hottest channel temperature of each device for the 25W of output power is less than 105°C (the bottom temperature of the micro-package is referenced to 70°C).

III. EXPERIMENTAL RESULTS

The measured performance of the packaged power amplifier under CW signal excitation is shown in figure 7.

The output power is 44dBm at 2dB of gain compression with a linear gain of 11.5dB and the associated PAE from 50% to 52% over the frequency range of 3.6-3.9GHz (biasing condition: V_{ds}=6V). These measurements do not take into account the losses of the test jig (Input / output insertion loss of the test jig ≈ 0.2dB).

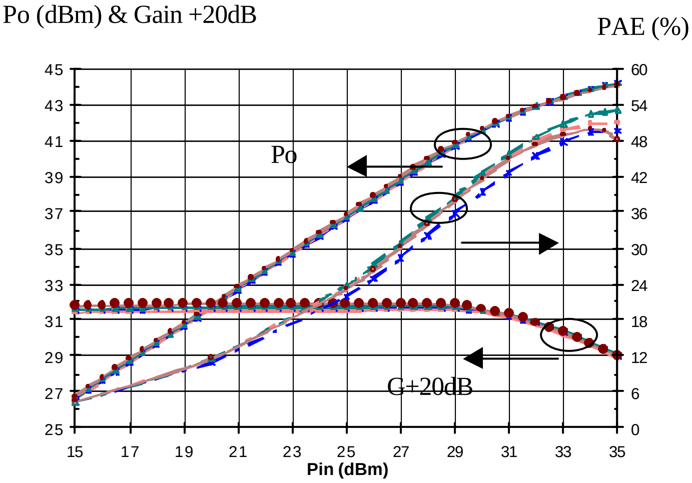

Fig.7: Measured Po, Gain+20dB, and PAE (Freq.=3.6-3.9GHz)

IV. CONCLUSION

The use of power PHEMT devices and hybrid technology allows to achieve the best output power and PAE with good linearity with a minimum weight and size of the power amplifier.

Using the comprehensive methodology developed by Alcatel, linear and non-linear electrical models of PHEMT chip devices were established. This work has allowed us to design a power amplifier at C-band for space application.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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