

# A computationally efficient approach for the design of RF power amplifiers

R.Paganelli, A.Santarelli\*, G.Zucchelli \*, A.Costantini\*, G. Vannini\*\*, F. Filicori\*

CSITE-CNR - Viale Risorgimento 2, 40136 Bologna, Italy, e-mail: rpaganelli@deis.unibo.it

\* DEIS, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy

\*\* Department of Engineering, University of Ferrara, Via Saragat 1, 44100 Ferrara, Italy

*A computationally efficient procedure for the design of RF power amplifiers is presented. The proposed approach allows for the identification of “near-optimal” source and load terminations of the amplifier stage providing maximum output power under assigned linearity, minimum gain and other possible constraints. The design procedure is completely based on closed form numerical computations, without requiring non linear optimisations as normally happens in standard design approaches. A single-stage 2.4 GHz amplifier prototype has been designed and manufactured in Silicon BJT MMIC technology, according to the criteria provided by the new methodology. Experimental results are in good agreement with simulations and confirm the validity of the proposed approach.*

## INTRODUCTION

Modern broad-band digital radio systems are increasingly demanding for highly linear, highly efficient RF power amplifiers. In particular, spectrally-efficient modulations, needed to face strong limitations in frequency band resources, are usually non-constant envelope schemes requiring challenging linearity constraints from RF power amplifier final stages. On the other hand, low cost, compactness and low power dissipation can only be achieved by means of highly efficient amplifying circuit solutions.

The identification of source and load terminations of an amplifier stage on the basis of standard approaches (1-7) is typically carried out within CAD programs through non linear numerical optimisations, aimed at the satisfaction of the assigned performance constraints. However, since non linear optimisation algorithms suffer from problems, such as multiple local minima and strong dependency on the initial guess solution, rarely this procedures lead directly to near-optimal designs.

An alternative approach for achieving linear operation of power amplifiers consists in limiting the input signal power level to such an amount so as specification requirements are satisfied (“back-off”). This approach is obviously scarcely efficient usually involving a loss in power-added-efficiency and consequently an increase of the device internal temperature.

Source- and load-pull measurements (8) are a possible alternative to standard design methodologies based on simulations, but unfortunately they require expensive equipments not usually available in most research and industrial laboratories. Moreover, source/load-pull techniques are just a way of empirically determining the

device response under particular operating conditions, without providing any model-like predictive capability.

In the paper, a new design procedure is presented, completely based on closed form numerical computations, which allows for the determination of a “near-optimal” choice of the complex source and load terminations of the amplifier stage, providing maximum output power under assigned linearity and minimum gain constraints. The proposed design methodology has been adopted for the design of a class-A, Silicon BJT MMIC-technology prototype amplifier at 2.4 GHz. The experimental results presented in the paper confirm the validity of the proposed approach.

## POWER AMPLIFIER DESIGN

Let us consider the amplifier schematic presented in Fig.1, where incident and reflected waves ( $50\Omega$  normalization) are defined at the circuit sections of interest. The design problem consists in the determination of the two complex reflection coefficients  $\Gamma_S$ ,  $\Gamma_L$  providing maximum output power  $P_{OUT} = (1/2) \cdot |b_{OUT}|^2$ , corresponding to a particular input available power level  $P_{IN}^{av} = (1/2) \cdot |a_{IN}|^2$ , under assigned linearity, minimum gain, stability and other possible constraints. The two terminations are not set independently one to each other, since the optimum  $\Gamma_L$  search is obviously dependent on the choice of  $\Gamma_S$  and vice-versa. Then, the design algorithm should be able to look for the optimal solution of a non linear problem, over a search space involving five real independent variables. These can be chosen, for example, as:  $\{ |a_{IN}|, |\Gamma_S|, \angle \Gamma_S, |\Gamma_L|, \angle \Gamma_L \}$ , where  $\angle a_{IN} = 0$  has been arbitrarily assumed, since the circuit is time-invariant. Standard design approaches are usually based on non linear optimisations involving a large number of circuit analyses based on time-consuming harmonic balance algorithms.

The design approach proposed here exploits a suitable change of the independent variables search domain, provided that the adopted non linear dynamic device model is defined by non linear equations explicitly describing the currents as function of the voltages at the intrinsic device ports. The Gummel-Poon BJT model<sup>1</sup>, conventional quasi-static FET models and different types of look-up-table based non linear dynamic models (9-10) meet this requirement. The new procedure is based on the adoption of a different set of independent variables, involving the phasors  $V_1$ ,  $V_2$  of the first harmonic of the voltages at the intrinsic transistor. In particular, the search for the optimal amplifier design is carried out in the space of the variables:  $\{ |V_1|, |A_V|, \angle A_V \}$ , where  $A_V = V_2/V_1$ . Without loss of generality,  $\angle V_1$  is here assumed to be zero.

This design space is convenient, since the port voltages  $V_1$ ,  $V_2$  completely define, without requiring any iterative procedure for solving harmonic balance equations, the large-signal transistor operation through the model equations, which explicitly provide all the corresponding harmonic components  $I_1^{(K)}$  and  $I_2^{(K)}$  of the currents and consequently, for a given parasitic network, the corresponding value of the load impedance  $Z_L$  or the load reflection coefficient  $\Gamma_L = (Z_L - R_0)/(Z_L + R_0)$ . The source reflection coefficient  $\Gamma_S$ , instead, is not univocally defined at the fundamental frequency by the transistor large-signal operating condition defined by the design variables:  $V_1$ ,  $V_2$ , or equivalently:  $|V_1|$ ,  $|A_V|$ ,  $\angle A_V$ . However, for any possible choice of  $|V_1|$ ,  $|A_V|$ ,  $\angle A_V$  the search for the optimal value of  $\Gamma_S$ , which minimizes the amplifier non-linearity under given constraints on minimum gain and stability, can be easily carried out by solving simple linear equations.

It should be noted that in the proposed design approach the higher order harmonics of the intrinsic transistor voltages are practically neglected, by assuming zero amplitudes. This could be considered as a simplifying assumption reasonably acceptable in quasi-linear class-A operation. However, the same assumption could be made also for different operating conditions (e.g., class-AB or B), which involve stronger harmonic distortion. In such cases, neglecting higher order voltage harmonics at the intrinsic transistor would correspond, instead, to a possible sub-optimal choice of harmonic source/load terminations, where the input and output matching network are designed to provide “shorts” at the harmonic frequencies. In practice, this is a possible way to avoid power transmission at unwanted harmonic frequencies.

According to the flow-chart presented in Fig.2 describing the proposed approach, a search for

<sup>1</sup> Gummel-Poon model equations define an explicit relationship between intrinsic device current and voltages provided that a simply linear parasitic base resistor is assumed.

increasing values of  $|V_1|$  is carried out for each couple  $\{ |A_V|, \angle A_V \}$  over a rectangular suitably-dense grid of values. The two phasors  $V_1$  and  $V_2$  imposed at each loop iteration, explicitly define the load reflection coefficient  $\Gamma_L$ , since the corresponding device current harmonic phasors must satisfy the voltage-controlled device model equations. Instead, univocal determination is not possible for the input termination  $\Gamma_S$  at the fundamental harmonic, due to the presence of the input signal source. Moreover, different values of  $\Gamma_S$  correspond to very different power amplifier performances, so that a nested search for the  $\Gamma_S$  value optimising the assigned design goals (i.e., minimize non-linearity under assigned constraints on minimum acceptable gain, stability, etc.) is carried out over a rectangular grid of  $\{ |\Gamma_S|, \angle \Gamma_S \}$  values. In particular, at the end of each loop in  $|V_1|$ , an upper limit  $|V_1|_{LIM}$  is found, beyond which no value of  $\Gamma_S$  exists, which can satisfy the design specifications on linearity. Once the  $\{ |A_V|, \angle A_V \}$  rectangular domain has been completely explored, suitable design maps can be drawn, where any desired large-signal performance index, such as output power, minimum requested gain, non-linearity indexes, network physical consistency indexes, stability margins, can be plotted over the bi-dimensional domain  $\{ |A_V|, \angle A_V \}$ .

In such a context, a power amplifier non-linearity index definition can be given in order to take into account both AM/AM and AM/PM amplifier distortion. In particular, we define a transfer function compression index as:

$$\varepsilon = \left| \frac{H - \hat{H}}{H} \right|$$

where:  $H = b_{OUT} / a_{IN}$  represents the complex ratio between the reflected wave  $b_{OUT}$  at the load section and the incident wave  $a_{IN}$  at the source section under small-signal conditions and  $\hat{H} = b_{OUT}^{(1)} / a_{IN}^{(1)}$  is the corresponding ratio between the first harmonic components of  $b_{OUT}$  and  $a_{IN}$  under actual large-signal conditions. It is interesting to observe that the above defined index can be related to the conventional third-order intercept point, providing the important advantage of transforming a power amplifier design specification on maximum (two-tone excitation) intermodulation distortion into an equivalent specification on a (single-tone excitation) complex gain compression.

Under the simplifying assumption of lossless input and output matching networks, the two quantities  $H$  and  $\hat{H}$  can be evaluated at each loop iteration by the following expressions:

$$H = \frac{\sqrt{1 - |\Gamma_S|^2} \cdot e^{j\varphi_{IN}} \cdot \sqrt{1 - |\Gamma_L|^2} \cdot e^{j\varphi_{OUT}} \cdot S_{21}}{1 - \Gamma_S \cdot \left( S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right)} \cdot \frac{S_{21}}{1 - S_{22}\Gamma_L}$$

$$\hat{H} = \frac{\sqrt{1-|\Gamma_S|^2} \cdot e^{j\varphi_{IN}} \cdot \sqrt{1-|\Gamma_L|^2} \cdot e^{j\varphi_{OUT}} \cdot b_2^{(1)}}{1 - \Gamma_S \cdot \frac{b_1^{(1)}}{a_1^{(1)}}} \cdot \frac{b_2^{(1)}}{a_1^{(1)}}$$

where:  $\varphi_{IN}$ ,  $\varphi_{OUT}$  are phases delays depending on the actual realisation of the input / output matching networks (irrelevant to the aim of evaluating the non-linearity index  $\epsilon$ );  $S_{ij}$  ( $i,j=1,2$ ) are the transistor small-signal scattering matrix elements;  $\Gamma_S$ ,  $\Gamma_L$  are the actual guess of the source and load transistor terminations and, finally,  $a_1^{(1)}$ ,  $b_1^{(1)}$ ,  $b_2^{(1)}$  are the first harmonic components of incident / reflected waves at the transistor ports. The latter can be easily evaluated for each choice of  $\{ |V_I|, |A_V|, \angle A_V \}$  on the basis of the intrinsic transistor model prediction of currents and the known linear parasitic network.

## EXPERIMENTAL VALIDATION

The consistency of the proposed power amplifier design method and the validity of the involved simplifying assumptions were preliminary explored by comparison with accurate Harmonic Balance simulations carried out by means of commercial CAD tools. To this aim, a single-stage 2.4-GHz quasi-linear power amplifier test circuit, based on Silicon BJT MMIC-technology by ST-Microelectronics, was designed, manufactured and tested. The Gummel-Poon model for the selected device was extracted on the basis of measured DC characteristics and S-parameters up to 20 GHz. Moreover, a bias condition for a power amplifier working in class A was chosen.

As shown in Tab.I, the complex transfer function  $\hat{H}$  and the non-linearity index  $\epsilon$ , corresponding to the  $\Gamma_S$ ,  $\Gamma_L$  identified by the proposed procedure at  $P_{OUT} = 18dBm$ , are in good agreement with the corresponding quantities obtained by means of Agilent ADS, without neglecting higher order voltage harmonics at the intrinsic transistor ports. Moreover, HB simulations, carried out by slightly varying the values of the source and load terminations  $\Gamma_S$ ,  $\Gamma_L$  around the choice found according to the proposed approach (Tab.II), clearly show that the obtained solution really correspond to a near-optimum power amplifier design.

A low-pass circuit topology for the input and output matching networks was adopted according to Fig.3, allowing for the biasing of the active device through the on-wafer RF probing system. The power amplifier prototype, manufactured by STM (Fig.4), was then measured both under small-signal (Fig.5) and large-signal (Fig.6) conditions. The good agreement between experimental results and circuit simulations, based on the Gummel-Poon BJT model, confirms the validity of the proposed approach.

## ACKNOWLEDGEMENT

This work was partly supported by the Italian National Research Council under the MADESSII project. The authors would like to thank the ST Microelectronics staff (Catania, Italy) for their technical support in the power amplifier layout design.

## REFERENCES

- (1) G.Gonzales, *Microwave Transistors Amplifiers-analysis and design*, 2nd Edition, Prentice Hall, 1997
- (2) S.C.Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, 1999.
- (3) L.A.Larson, *RF and Microwave Circuit Design for Wireless Communications*, Artech House, 1997.
- (4) J.L.B.Walker, *High Power GaAs FET Amplifiers*, Artech House, 1993.
- (5) F.Giannini, G.Leuzzi, E.Limiti, J.S.Mroz and L.Scucchia, *Nonlinear Mixed Analysis/Optimization Algorithm for Microwave Power Amplifier Design*, IEEE Trans. on MTT, Mar. 1995.
- (6) J.S.Snider, *A Theoretical Analysis and Experimental Confirmation of the Optimally loaded and Overdriven RF Power Amplifier*, IEEE Trans. on ED, Dec. 1967.
- (7) S.A.Maas, *Nonlinear Microwave Circuits*, Artech House, 1988.
- (8) G.Madonna, A.Ferrero, M.Pirola and U.Pisani, *Testing microwave devices under different source impedance values-a novel technique for on-line measurement of source and device reflection coefficients*, IEEE Trans. on IM, Apr 2000.
- (9) F.Filicori, A.Santarelli, P.Traverso and G.Vannini, *Electron device model based on nonlinear discrete convolution for large-signal circuit analysis using commercial CAD packages*, Proc. of GAAS99, Munich, Germany, Oct 1999.
- (10) D.E.Root et al., *Technology independent large-signal non quasi-static FET models by direct construction from automatically characterized device data*, Proc. of 21st EuMC, Sep 1991.

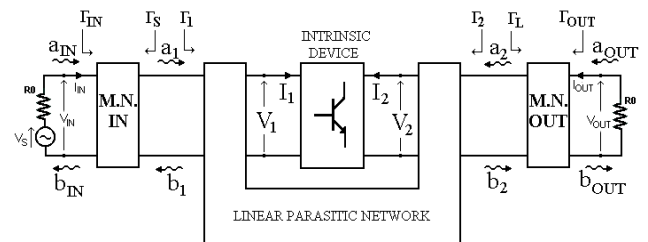


Figure 1: Single-stage power amplifier schematic (bias networks omitted)

	$ \hat{H} $ [dB]	$\angle \hat{H}$ [deg]	$\epsilon$ [%]
New design algorithm	17.5	122	5.0
CAD validation	17.5	123	5.1

Table I: Complex gain and non-linearity index corresponding to  $P_{OUT} = 18$  dBm. Values obtained under the simplifying assumptions adopted by the proposed design procedure vs. values obtained by means of Agilent ADS. As expected, negligible differences confirm the validity of the new procedure simplifying assumptions..

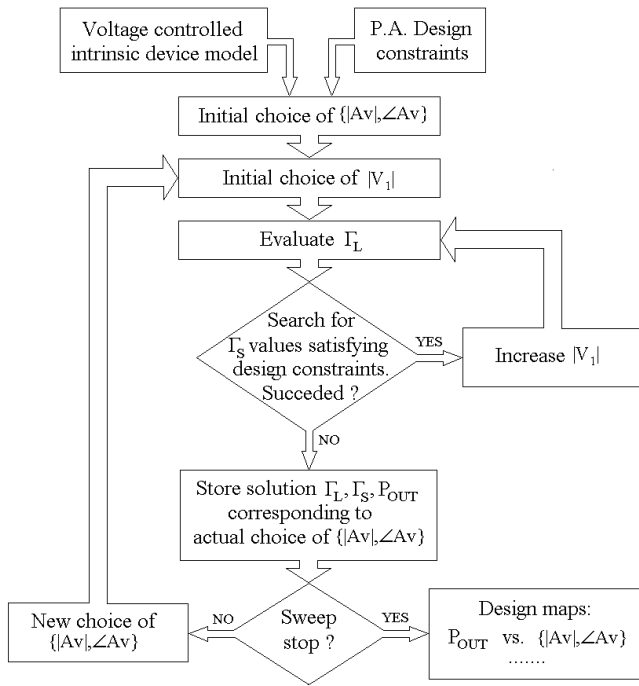


Figure 2: Flow-chart of the proposed power design approach.

$\Delta Z_S$ [ $\Omega$ ]	$\Delta Z_L$ [ $\Omega$ ]	$P_{OUT}$ [mW]	/H/ [dB]
—	—	61.8	17.5
—	2	60.4	17.1
—	-2	60.6	17.8
—	j2	60.5	17.5
—	-j2	61.6	17.3
2	—	60.3	17.1
-2	—	65.3	16.8
j2	—	58.8	19.1
-j2	—	63.1	15.5

Table II: HB results ( $\epsilon = 5\%$ ) obtained by slightly varying the source/load impedances with respect to the near-optimum values:  $Z_S = (4.364 - j 3.120) \Omega$ ,  $Z_L = (12.505 + j 1.712) \Omega$ . Nominal solution (first row) satisfies the minimum requested small-signal gain equal to 17 dB.

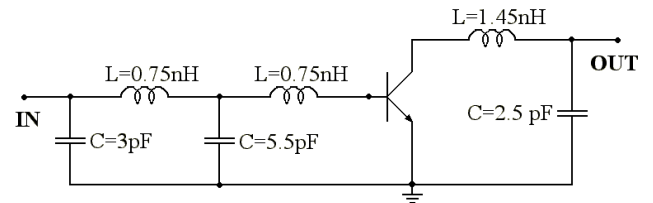


Figure 3: Circuit schematic of the power amplifier prototype working at 2.4 GHz designed for  $\epsilon = 10\%$  at  $P_{OUT} = 20$  dBm.

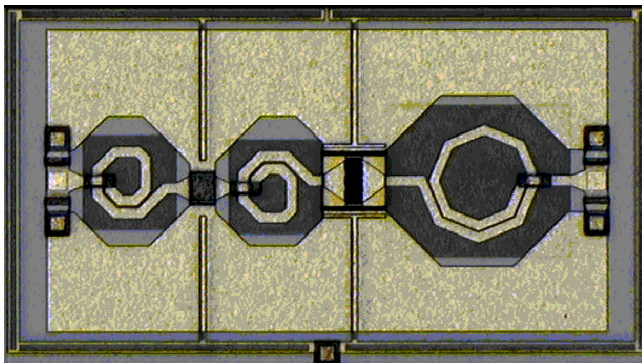


Figure 4: Photograph of the power amplifier prototype manufactured by ST Microelectronics.

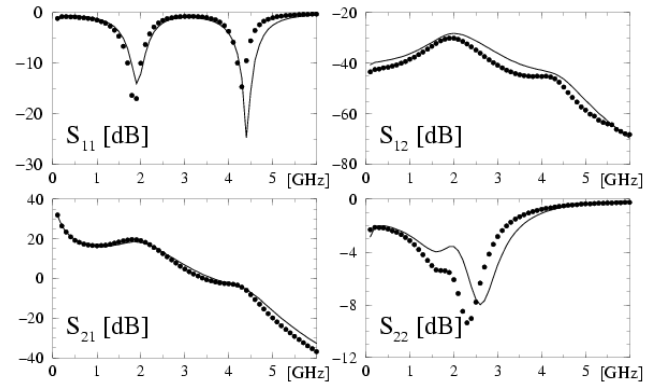


Figure 5: S-parameters of the power amplifier prototype. Measurements ( $\bullet$ ) versus predictions ( $—$ ).

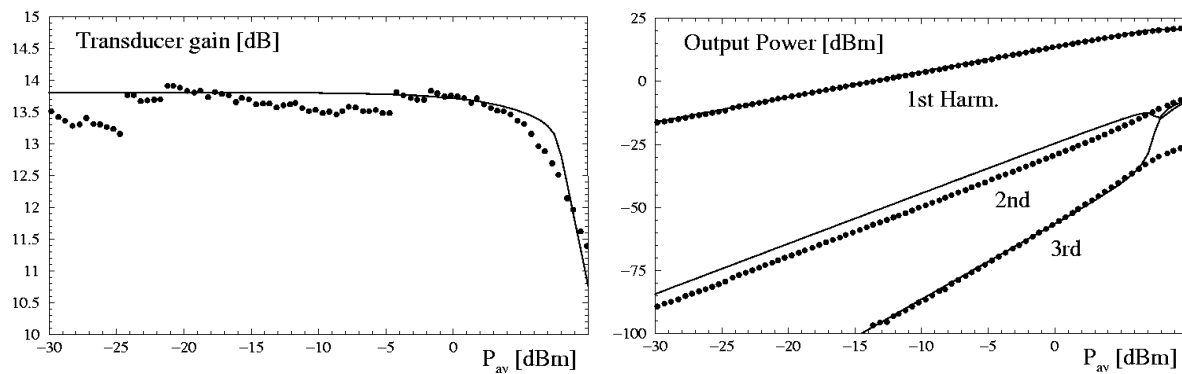


Figure 6: Transducer gain (left) and harmonic distortion (right) of the power amplifier prototype. Measurements ( $\bullet$ ) versus predictions ( $—$ ) obtained through the Gummel-Poon BJT model.