Fully-integrated wideband TTD core chip with serial control

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The design and performance of a fully-integrated wideband TTD core chip is presented. The integration philosophy is discussed. The MMIC presented integrates 7-bit amplitude and 6-bit time-delay, as well as the control functions of a transmit/receive module. This control includes a serial-to-parallel converter with TTL-compatible input. The MMIC is realised on the 0.25µm PHEMT (ed02ah) process of OMMIC.

INTRODUCTION

In the next generation Transmit/Receive (T/R) Modules for phased-array antenna applications, cost reduction and performance enhancement are of vital importance. By using microwave monolithic integrated circuits, these demands can often be met. Phased-array antennas use up to thousands of T/R modules containing several functions. An example of such a T/R module is shown in Figure 1, which is based on the partially common-leg architecture. The volume available for these transmit/receive modules is very limited, considering λ/2 element spacing and the trend towards smart skins.

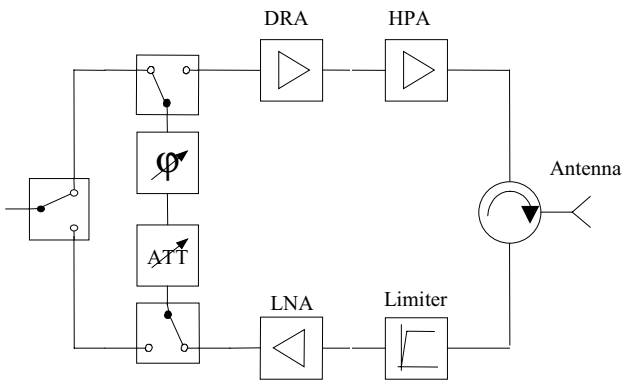

Figure 1: Block diagram of next generation T/R modules.

The bandwidth for new apertures is increasing all the time. Over the years, the systems have evolved from narrowband single-function systems via wideband single-function sytems into wideband multifunction systems that pose even more stringent requirements on the bandwidth. The steering of these systems is still based on setting the required time delay per module by approximating it with a phase difference which is supposed to hold over the required instantaneous bandwidth. However, the newest systems, require even wider relative instantaneous bandwidths, whilst at the same time they are dealing with large arrays and with a large maximum scan angle. In order to let the pointing error due to the phase steering be smaller than half the antenna beam width, the relative bandwidth, maximum scanning angle and array size are related through [1]

$$\frac{\Delta f}{f} = 0.886 \frac{\lambda}{L \sin \Theta},$$

where Δf: bandwidth,
f: frequency
Θ: maximum scan angle
L: array size,
λ: wavelength in free space

As an example, 20% relative bandwidth for a 20 element λ/2-spaced antenna will be limited to 30° scanning from boresight.

It is for this reason that true-time delays are required for phased-array control. Given the volume constraints mentioned above, it is often not feasible to realise these time delays in conventional ways such as stripline. The approach taken in this work is to integrate all core chip functionality on a single MMIC. This functionality includes TTD and gain control, amplification, transmit/receive switching and the necessary control logic, including a serial-to-parallel converter.

To the knowledge of the authors, it is for the first time that such a wideband TTD core chip is presented.

CORE CHIP DESIGN

The topology of the core chip is illustrated in Figure 2 below. Much attention was paid to a proper gain distribution. A lot of gain is needed to compensate for the losses associated with the TTD elements. The gain was distributed such that the resulting P_{1dB} was optimal, based on identical two-stage amplifiers. The TTD and attenuator core of the chip is switched between transmit and receive by means of two identical T/R switches, based on a series and parallel FET per leg. The digital control is equivalent to the control described in [2], although the actual implementation is different.

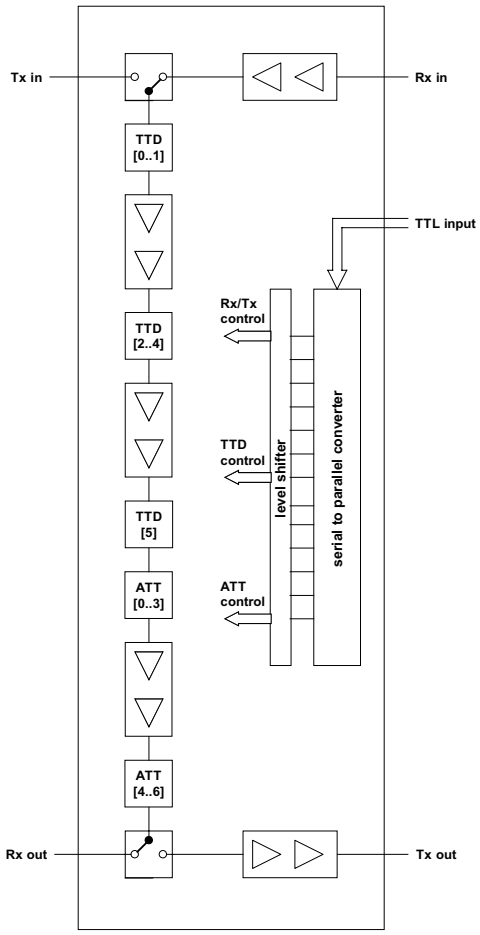

Figure 2: Block diagram of the TTD core chip.

TTD and attenuator bits

The core of the MMIC is formed by 6 TTD bits and 7 attenuator bits. The minimum time delay required is determined by the beam width of the antenna employed and was 2.5 ps for our application. 6 bits with a binary distribution were employed, the maximum time delay was therefore just below 150 ps, which is equivalent to approximately 45 mm in free space. The TTD bits are based on constant-R networks. Due to the maximum operating frequency, the maximum time delay of such a network is below 20 ps [3]. The three smallest bits could be based on the self-switched topology, the three biggest bits are based on the SPDT topology. The two biggest bits were realised by cascading more constant-R networks. The attenuator bits are based on switched pi attenuators, more details can be found in [4].

Wideband amplifier

The wideband amplifiers used in the core chip were designed mainly to compensate for the high TTD losses. Also for this reason they were designed to have a positive gain slope of 7-13 dB with frequency since the TTD's generate a negative slope. The design bandwidth was 2-18 GHz. Five two-stage amplifiers are used in the core chip, the distribution can be found in Figure 2. All gain cells are equal (due to the wideband nature, individual designs were not feasible). For this reason, the design was a compromise between linearity and noise performance. It was designed to have a noise figure of 4.3 dB and a P_{1dB} at the input of 5dBm.

LAYOUT

The multifunction chip is realised in the 0.25µm PHEMT (ed02ah) process of OMMIC. A photograph of the chip is depicted in Figure 3.

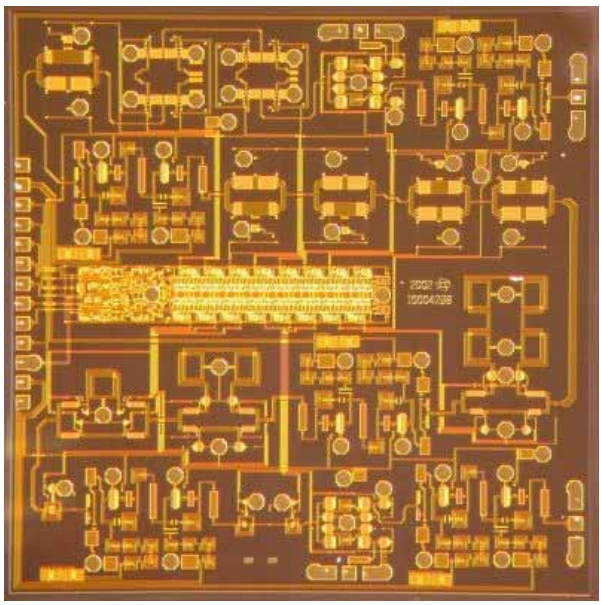

Figure 3: Photograph of the TTD core chip.

MEASUREMENT RESULTS

This section shows the measurement results of the TTD core chip. In Figure 4, gain and input and output return losses are shown. The gain in transmit mode is not shown, but is approximately 3 dB lower.

The attenuator and TTD control are illustrated by the major state behaviour in Figures 5 and 6 respectively and by their respective frequency planes in Figures 7 and 8.

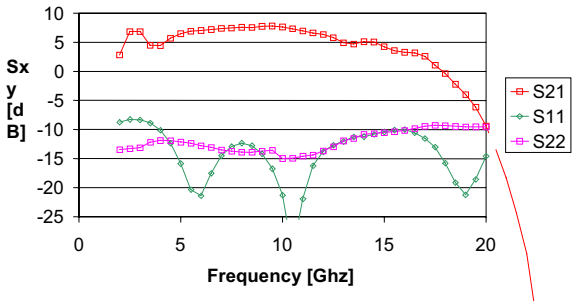

Figure 4: The measured S11, S21, and S22 in receive versus frequency for the TTD core chip

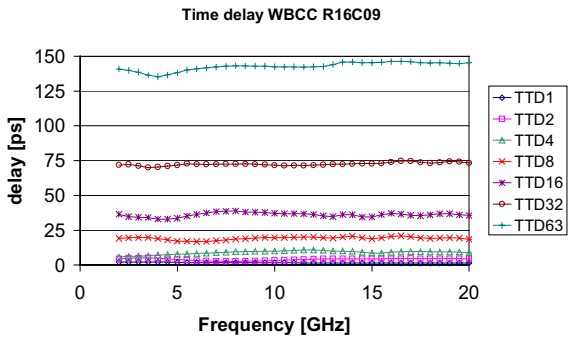

Figure 5: The measured major TTD states versus frequency for the TTD core chip.

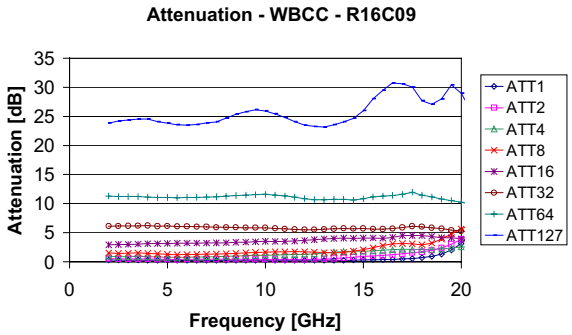

Figure 6: The measured major attenuator states versus frequency for the TTD core chip.

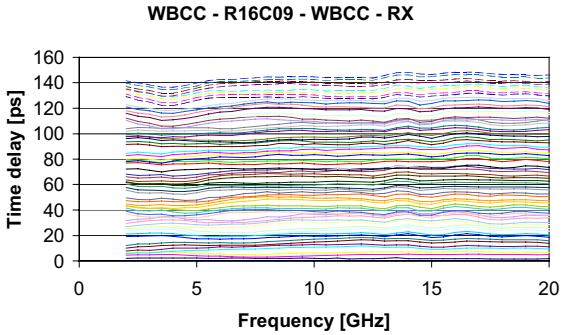

Figure 7: The measured TTD- frequency plane for the TTD core chip..

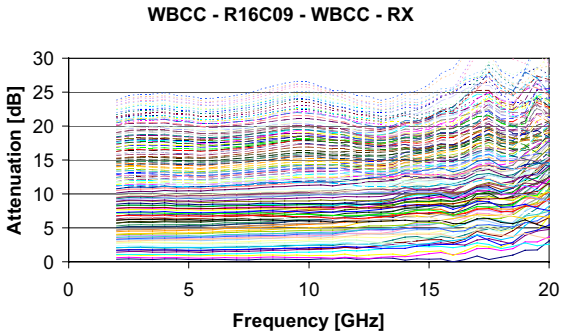

Figure 8: The measured attenuation- frequency plane for the TTD core chip.

From the TTD-frequency and attenuation-frequency plane, it was concluded that the behaviour shows no significant gaps and hence is capable of an operating bandwidth of 3-16 GHz.

Figures 9 and 10 show the transducer gain for the receive and transmit path. These measurements were performed at several frequencies, due to the wideband nature of the design. The vertical bars indicate the 1-dB compression points.

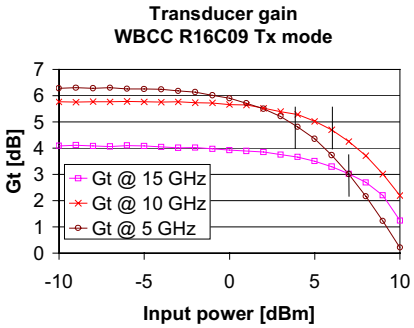

Figure 9: The measured transducer gain versus input power for the TTD core chip in the transmit mode.

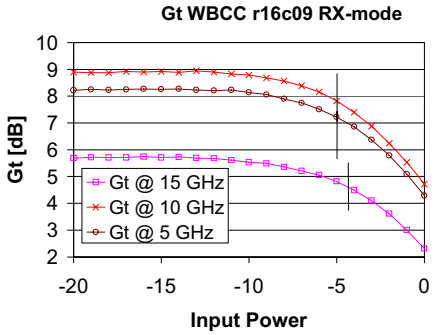

Figure 10: The measured transducer gain versus input power for the TTD core chip in the receive mode.

CONCLUSION

The design of a fully-integrated wideband TTD core chip is successfully accomplished. Despite a very high functional integration and a very compact layout, the MMIC was functional in a single iteration. The level of integration makes this chip extremely suitable for a two chip T/R module solution for versatile phased-array systems. It can be used in applications with ultra-wideband requirements and hence may prove useful in shared or multi-function apertures, as well as in EW arrays.

REFERENCES

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