E/D pHEMT Multi Frequency Generator GaAs MMIC for Aerospace Applications

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***Abstract* — This paper presents the design and performance of a multi frequency generator MMIC to be used in transmit/receive modules for S band transponders. The technology used is a European commercial Enhancement/Depletion (E/D) pHEMT process, compatible with low noise reception. Quasi-monolithic Voltage Controlled Oscillator (VCO), divide-by-four digital frequency divider, active frequency multiplier-by-three and relative power dividers and buffers have been integrated into a single chip to generate all the system frequencies in a flexible architecture.**

Measured phase noise of the VCO depends on the external resonator and varactor used. Values of –105dBc/Hz@100KHz have been measured with external high Q resonator which is comparable to best performance reported of GaAs based VCOs. The frequency divider by four has an operating window from 30 MHz to >4GHz and an output power of more than 4 dBm. Multiplier by three provides more than 5 dBm in each of the two outputs with adjustable level of harmonics.

I. Introduction

The use of MMIC has drastically changed the design of electronic equipment. This is especially true for satellites and space modules asking for complex transmit/receive circuits with very stringent requirements. They have permitted a reduction in mass and cost by a factor of 2 from the previous employed discrete hybrid family [1] , not only keeping but also increasing the reliability of equipments. Transceiver subsystems using MMIC chips have been recently developed for communication applications. However the multiple MMIC chip assembly solution results in greater manufacturing and tuning time, resulting in higher cost. Current MMIC technology offers solution to this problem allowing the integration of many functions on a single chip without a big impact on yield and performance, therefore reducing the number of chips and resulting in a lower test and module assembly cost. However the number of circuits and the area of the chip must be carefully chosen to optimise heat dissipation and minimize the effect of wafer variability, which can degrade the yield of the process and cancel the advantages of size reduction

The developed MMIC has the function of coherent generation of different frequencies and can be flexibly used in transmit and receive modules designed especially for Telemetry, Tracking, and Control (TTC) of satellite systems. In addition to the VCO, the frequency tripler and the other analogue functions, a digital divider has been inserted to allow the use of this mixed analogue/digital chip in PLL systems. However the output power level of the divider is capable of providing a local oscillator signal, if necessary.

II. Fabrication Process

There are no technologies that are ideal for all requirements. IC design demands many tradeoffs in performance and many factors have been considered at the moment of starting the design of a custom MMIC, taking into account the application for which the chip is developed.

The very strict spatial requirements ([2],[3]) are probably the most limiting factor. Space radiation effects have to be considered in the design of a circuit to be used in aerospace systems. The so-called Single Event Effects (SEE) associated with the transit of heavy ions through semiconductor junctions have to be minimized to reduce failure risk. The most dangerous of this kind of effects is the Latch-up (SEL, [4]) which can lead to the destruction of the device and has to be completely avoided. In this sense GaAs devices, which are not prone to SEL, seemed a good choice. Thinking on a deeper level of integration (i.e. the entire transmitter/receiver) as is the case of our design, compatibility with LNA design and with the realization of both digital and analogue circuitry has to be considered. Finally, the technology should be preferably European and accessible to external designers (i.e. universities).

The chosen process is a commercial foundry process from OMMIC in France, developed specifically for low noise applications up to 70GHz. The active pseudomorphic GaInAs layer is grown by Hetero-Epitaxy and the pHEMT transistors have a gate length of 0.2µm with an f_T=60GHz. The process is suitable for the implementation of both digital and analogue functions and it is at present under space qualification.

III. System Overview

A block diagram of the MMIC is showed in Fig 1. The selection of the three main functions (oscillation, frequency multiplication and division) was motivated by the use for which the chip is intended: the generation of all the system frequencies used in a transmit or receive module at S-band. Quasi-MMIC VCO was chosen instead

of a fully integrated solution to enhance the flexibility required by the circuit. The tank resonant circuit outside the chip gives a degree of freedom (and even better performance) which is not possible if the varactors and resonator were included on chip.

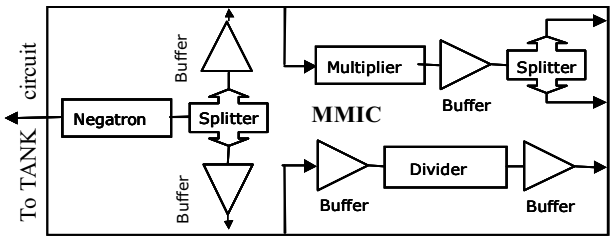

Fig. 1. Block diagram of the frequency generator MMIC

As can be noted, each of the elementary functions presents two or more input/output terminals to access the circuit from the outside. This solution has been adopted to facilitate the first on wafer testing (to reject possible non compliant components, therefore reducing module assembly cost) and to allow different system configurations through appropriate connections.

Two possible configurations in transmission and reception are illustrated in fig. 2 and 3. Additional functionalities have not been integrated to make possible the use of a single chip in both types of modules, so reducing the production cost.

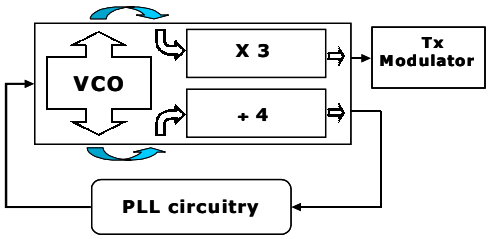

Fig. 2. Configuration for use in a transmit module

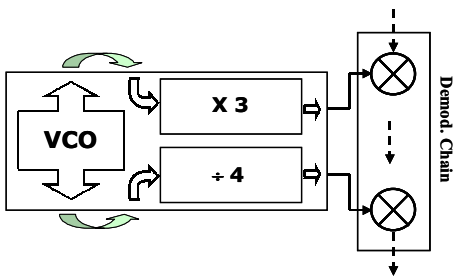

Fig. 3. Configuration for use in a receive module

IV MMIC Design and Measurement

The first prototype (Fig. 4) has a chip area of 4x5mm^2 to allow individual and collective characterisation of the functions and separate bias to check possible DC power reduction. Next prototype is supposed to be a more compact chip (around 75% of actual size). An option integrating the VCO with a LNA and a Mixer on the same MMIC is also considered.

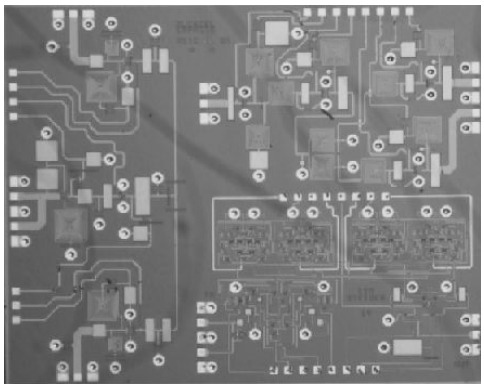

Fig. 4. Photograph of the circuit. (Layout area: 4x5 mm^2)

A. Oscillator Circuit

The VCO consists of an external resonator, fully flexible to configure, and an integrated negatron plus a buffer, a power splitter and two output buffers.

It is important to notice that the varactor tank circuit is outside the chip [5]. The negatron uses a transistor with the source capacitively coupled to ground. To simplify the biasing scheme the active device is self-biased. The output is taken from the drain and the tank circuit is connected to the gate of the transistor. This solution achieves better isolation between the output and the resonant circuit. With this configuration, just one pin of the chip is required to connect the tank circuit to the gate of the transistor.

The first buffer was designed to provide excellent isolation in order to achieve good frequency pulling at the VCO. The power splitter consists simply of a resistive splitter occupying minimum area. The output buffers were designed to provide high isolation and good output matching to interface with a 50Ω system.

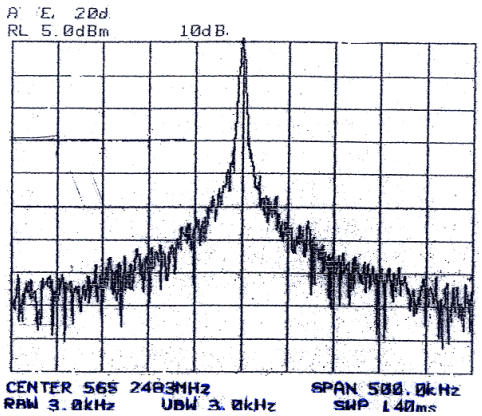

Fig. 5. Measured spectrum of the free running VCO (Fosc≈ 560MHz) at a tuning voltage of 0V. Measured phase noise is approximately –105dBc/Hz @ 100 KHz

The negatron is able to provide negative resistance in a band in excess of 1 GHz around 700 MHz. The whole circuit delivers more than 5 dBm at each output with the frequency bandwidth depending on the resonator used. It requires a DC bias of +3.5V and 47mA. In Fig. 5 is shown the measured performance at 560 MHz with an external coaxial resonator. Measured phase noise of –

105dBc/Hz@100KHz is similar to the values obtained with Si-MMIC using the same resonator configuration [5], and it is not far from the phase noise achieved with BiCMOS technology [6].

B. Frequency Multiplier

The frequency multiplier consists of a tripler [7], a buffer, a power splitter and two output buffers. The tripler is basically a pHEMT that works as a harmonic generator. Its biasing point was optimized to obtain the maximum third harmonic power. This block also includes a resonant circuit to attenuate the first and second harmonics. The first buffer ensures enough output power to drive the splitter. The latter is a Wilkinson power divider designed to contribute to the attenuation of the fourth and higher harmonics. Finally, the output buffers were designed to ensure good isolation and output matching.

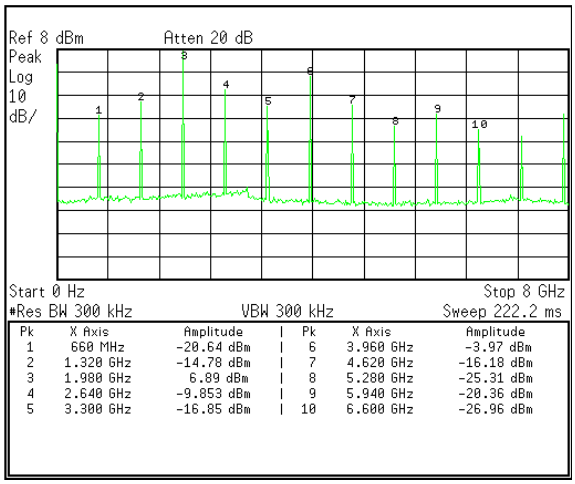

Fig. 6. Measured output spectrum of the multiplier (Fin=660 MHz)

The measured output power is greater than 5 dBm with more than 18% bandwidth around 710 MHz at an input power of 5 dBm. Fundamental frequency is 28dB and 2nd harmonic 22dB below the desired signal right at the output of the MMIC (Fig.6). The level of other unwanted harmonics can be further decreased with external filtering. DC bias requirements at the maximum output power are +3.5V and 38.5 mA. Bias of the output buffers can be adjusted to trade off harmonic contents at the output and DC power consumption.

C. Digital Frequency Divider

The circuit consist of two cascaded master slave D flip-flops with feedback from the inverted output. (Fig. 7). Input and output differential buffers have been inserted to interface the circuit with the conventional 50Ω systems. The inner frequency divider is designed to operate with a differential input, and a couple of source follower stages are employed to provide the necessary level shift between the two flip-flops and to enhance speed. The basic cell is implemented using source coupled FET logic (SCFL ,[8],[9]).

A detailed step by step procedure has been applied to the election of transistor sizes and bias, to maximize efficiency, to keep HEMTs in saturated region and to adjust delays during the high-low transitions at each one of the three different transistor levels present in the SCFL cell. DC inverting curve was obtained as a first approach. In a further step dynamic inverting transfer characteristic was optimized taking into account present signals at the other inputs.

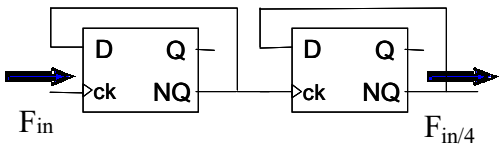

Fig. 7. Block diagram of the digital divider

Performance of the frequency divider was investigated in a 50-Ω system. Sensitivity was measured for the separate divider mounted on a chip carrier and is reported in Fig. 8. The circuit is capable to provide an output signal with more than 4dBm (depending on the output buffer biasing) with the input ranging from 80MHz to 4.5GHz and a sensitivity window wider than 30dBm. The total power consumption is 82mA @ -5.2V.

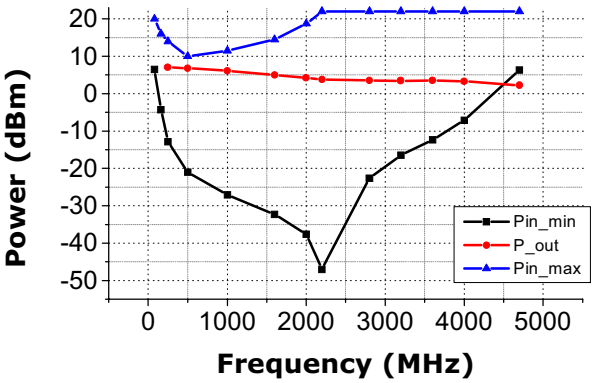

Fig. 8. Input sensitivity and output power @50 Ohm I/O

V. Conclusion

The design and implementation of a single chip VCO, multiplier and frequency divider, to be used in S-band transponder, have been presented. The new circuit offers a compact, flexible and efficient low cost solution for the generation of all the system frequencies in both transmit and receive modules.

The negatron is able to provide oscillation in a band exceeding 1 GHz and phase noise of -105dBc/Hz @100KHz, has been measured. A value which is similar to the one obtained with Si-MMIC using the same resonator configuration and it is not far from the phase noise achieved with BiCMOS technology. The multiplier by three provides two outputs with more than 5 dBm each and low spurious level. Frequency divider by four has an operating window from 80MHz to 4.5GHz with excellent

sensitivity and an output power higher than 4 dBm in the whole frequency band.

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