A 10 Gb/s CMU in SiGe BiCMOS commercial technology with multistandard capability

Francesco Centurelli *, Alessandro Golfarelli §, Jesus Guinea, Leonardo Masini §, Damiana Morigi §, Massimo Pozzoni, Giuseppe Scotti *, Alessandro Trifiletti *

STMicroelectronics, I-20010 Cornaredo (MI), ITALY
* Dipartimento di Ingegneria Elettronica, Università "La Sapienza" di Roma, I-00184 Roma, ITALY
§ Laboratori Fondazione Guglielmo Marconi, I-40044 Pontecchio Marconi (BO), ITALY

***Abstract* — A 10 Gb/s CMU has been fabricated in a commercial SiGe BiCMOS technology featuring multistandard compliance with SDH/SONET and 10 GbE specifications, dual reference clock frequency and output jitter below 80 mUIpp. The phase tracking loop uses a charge pump with low common mode current to minimize frequency ripple. Power supply is 2.5 and 3.3 V and the total power consumption is below 480 mW.**

I. Introduction

In recent years it has been observed a widespread diffusion of high bit-rate optical communication systems for both long distance telecom transport networks and short-haul datacom systems. Optical transmission technologies have completely taken over the backbone and transport network segments thanks to their unparalleled performance, and the advent of multimedia applications has spurred the demand for higher-capacity fiber-based LANs. 10 Gb/s is nowadays the highest bit-rate used in commercially available serial data links, and it is covered by different standards, both for long-distance telecom systems (SDH/SONET [1]-[2]) and for datacom LANs and MANs (IEEE 802.3ae-10 Gigabit Ethernet [3]).

Network components demand for low cost, high productivity, small size and low power consumption; for short-haul systems such as LANs and the access network in particular, an important consideration is cost competitiveness. In this scenario, the availability of multi-standard compatible building blocks can greatly contribute to cost and time-to-market reduction.

In this paper we present a SiGe 3.3 V 10 Gb/s Clock Multiplier Unit (CMU) IC that can be used with all the main standards for 10 Gb/s optical communications, i.e. SDH STM-64 / SONET OC-192 (9.953 Gb/s), SDH / SONET with forward error correction (10.664 Gb/s, 10.704 Gb/s) and IEEE 10 Gigabit Ethernet (10.3125 Gb/s). Section II presents the system-level design of the PLL clock multiplier unit, Section III describes the circuit design of the main building blocks, and Section IV gives some technological details and shows the results of measurements.

II. Clock Multiplier Unit System Design

The Clock Multiplier Unit (CMU) is based on a charge-pump phase-locked loop (CP-PLL) that works as a frequency multiplier to generate a low jitter 10 GHz clock signal from a low speed external reference clock. The PLL can generate frequencies from 9.9 GHz to 10.8 GHz, satisfying both the SDH/SONET and the 10 Gigabit Ethernet requirements; a 16/64 programmable feedback divider allows the use of two different families of reference clock sources: 155-167 MHz or 622-669 MHz.

The primary design goal for the CMU has been low jitter generation: SDH specifications impose an output jitter at the transmitter optical interface below 0.1 UIpp when integrated between 50 kHz and 80 MHz [2]. This jitter contains both electrical and optical components, the former including the generated jitter of the CMU and jitter generated in the transmitter chip and in the laser modulator driver: this requires a minimization of the CMU jitter. Since this chip was designed to be used in conjunction with other ICs that perform interfacing between SONET or 10 GbE signals, and not for serial-input / serial-output regenerator applications, SONET jitter transfer specifications are not relevant. The PLL was however designed to show peaking in the transfer function below 0.1 dB, making thus possible its application in a SONET repeater module, where the 120 kHz jitter transfer bandwidth could be achieved by using an additional low bandwidth PLL to generate the reference signal [4].

Two types of jitter components are important in PLL design: the jitter due to the noise sources internal to the PLL (VCO phase noise, filter noise) and the reference clock transferred jitter, that is the phase noise of the reference clock filtered by the PLL jitter transfer curve H(s). A small PLL bandwidth is recommended to limit the jitter coming from the clock reference source, whereas a large bandwidth can reduce the jitter generated inside the PLL, that is filtered by the high pass function 1-H(s). The PLL bandwidth has been chosen as a trade-off to minimize the sum of these contributions: the optimum bandwidth was found to be 2.5 MHz assuming crystal-based commercial low-jitter reference clock generators and an internal VCO phase noise of –85 dBc/Hz at 100 kHz offset from the carrier, and taking into account the filter noise. The jitter transfer function H(s) for a second order CP-PLL can be calculated as shown in [5] and in case the frequency of the zero is set to be much lower than the PLL bandwidth, the following

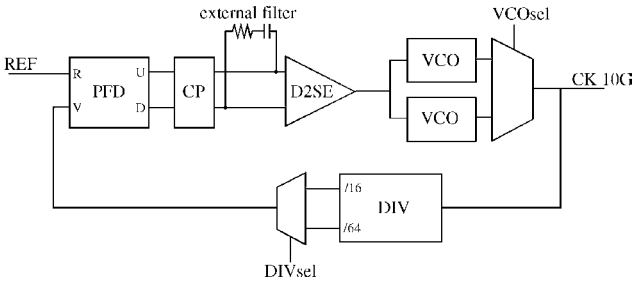

Fig. 1. CMU IC functional block diagram.

formula can be used to define the jitter transfer bandwidth BW:

$$BW = Av\ Kv\ Rz\ Icp / 2\pi\ N \qquad (1)$$

where Av is the gain of the voltage amplifier between the filter and the VCO, Kv is the VCO gain in Hz/V, Rz is the series resistance of the loop filter, Icp is the charge pump current and N is the feedback divider ratio. By changing the external resistance of the loop filter Rz, it is possible to keep the PLL bandwidth fixed when the divider ratio is changed from 16 to 64.

For what concerns jitter transfer peaking, the main sources can be found in the PLL phase margin and in the closed loop doublet. The presence of at least an additional pole, due to loop filter parasitic capacitances and to the voltage amplifier, makes the PLL a third order loop; a phase margin better than 60° is required to have a closed loop transfer function with less than 0.1 dB peaking, and this is obtained if the high frequency poles in the loop are at sufficient higher frequency than the PLL bandwidth. An additional source of peaking is the pole-zero doublet in the PLL transfer function, and its contribution can be estimated as [6]:

$$Pk_{dB}=20\log(1+f_z/BW) \qquad (2)$$

where f_z is the frequency of the RC filter zero. This peaking contribution is quite critical, since it could affect the peaking of the overall jitter transfer function if this CMU is used for a SONET repeater with a 120 kHz bandwidth PLL to generate the reference signal. A frequency of 15 kHz has been chosen for the zero, to minimize this contribution to the transfer function peaking.

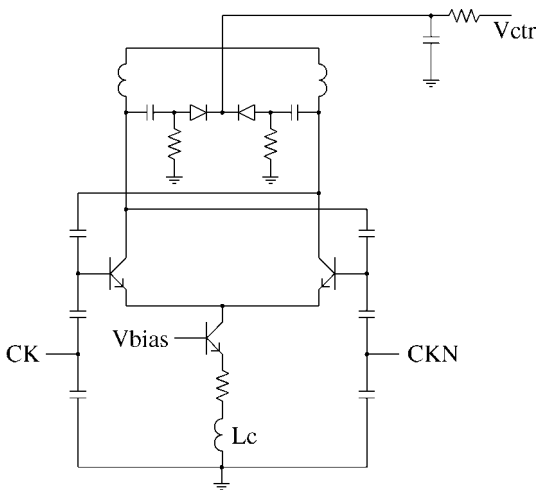

Fig. 2. Voltage-controlled oscillator.

III. CMU Circuit Design

The block scheme of the IC is shown in Fig. 1: the PLL consists of a VCO, a programmable 16/64 frequency divider, a phase- and frequency-detector (PFD), a differential charge pump (CP), a low-pass filter with differential to single-ended converter amplifier (D2SE). The generated clock signal is made available by a 50 Ω CML output buffer. The PLL is fully integrated except for the differential loop filter, which consists of an external resistor and capacitor series. Additional low-value capacitors have been added on chip to minimize high frequency ripple induced by current injection.

A. Voltage-Controlled Oscillator

To satisfy the jitter generation specification, the VCO has been implemented as an LC-tank bipolar VCO with capacitive tapping, as shown in Fig. 2 [7], to obtain a phase noise of –85 dBc/Hz at 100 kHz offset. Both the tank inductors and the current source choke Lc have been integrated as spiral inductors implemented in the top metal layer (2.5 μm thickness), and a patterned ground shield has been inserted below the inductors to reduce substrate losses : this reduces mutual coupling (compared to solid ground shielding) and the impedance to ground, providing a good short for the electric field [8].

VCO tuning is performed by means of two P+/Nwell varactor diodes, driven by the D2SE output: rail-to-rail swing is needed to maximize tuning range. To overcome the issue of the very limited tuning range (about 12 %) provided by the LC VCOs, two VCOs centered at 9.8 GHz and 10.45 GHz have been integrated on the chip, with the capability of selecting the desired one by means of a dedicated pin, while the unused one is switched off to prevent any interference. This allows the CMU to operate with the different standards for 10 Gb/s transmission over all process, supply voltage and temperature (PVT) conditions.

B. Frequency Divider

A CML semi-synchronous frequency divider has been used as a trade-off between phase noise performance and high speed requirements: a 6 dB phase noise improvement with respect to a fully asynchronous implementation has been obtained in simulation [9]. The architecture is shown in Fig. 3: an asynchronous three-stage prescaler divides by 8 the 10 GHz clock from the VCO; it is followed by a three-stage synchronous divider to get an overall division ratio of 64. An intermediate tap is available to choose a division ratio of 16, and the final frequency to the PFD is selected by the 2:1 multiplexer.

The D-type flip-flops (DFF) used in the prescaler have been designed using CML latches without emitter followers, to minimize power consumption and reduce the risk of on-chip ringing oscillations, that could affect the eye diagram. Transistor dimensions have been

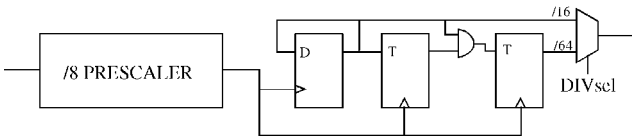

Fig. 3. Frequency divider block diagram.

optimized to reduce the propagation delay time, and smaller transistors have been used in the upper differential pairs to reduce parasitic capacitance without degrading the cut-off frequency. The design of T-type flip-flops in the synchronous section is based on the topology of the DFF; a feedback loop is closed from the output through a CML XOR gate to obtain the toggle function.

C. Phase-Frequency Detector

To minimize jitter, a tri-state PFD and charge pump have been used, that produce zero current between clock transitions. A standard three-state PFD in CML logic has been implemented [10], and to eliminate the dead-zone problem [11]-[12] a delay element has been introduced in the reset path, so that minimum width pulses are always present when the clock signals are in phase. A minimum pulse duration of 160 ps has been chosen to compensate the flip-flop finite rise/fall times and the charge pump finite activation time with a limited reduction of the linear range of the PD [13]. Moreover, this allows to minimize jitter, since minimum (differential) current due to device mismatch is integrated by the loop filter even when a low frequency reference crystal is used. A bipolar implementation has been preferred to a CMOS-based one to maximize device speed and so allow a short minimum pulse duration.

The D-latches use the topology in Fig. 4, where the principles of the low-voltage topology in [14] have been exploited to avoid adding a third stacked level for the reset input.

D. Charge Pump

The charge pump scheme is shown in Fig. 5; it has the same topology as the one in [15], but uses bipolar devices to provide a very fast turn-on time. To minimize jitter due to mismatches, the charge-pump currents are completely switched to the supply rail when the charge pump is switched off, so the common mode loop has to compensate only the average charge injected during minimum width pulses, resulting in a very small common-mode current.

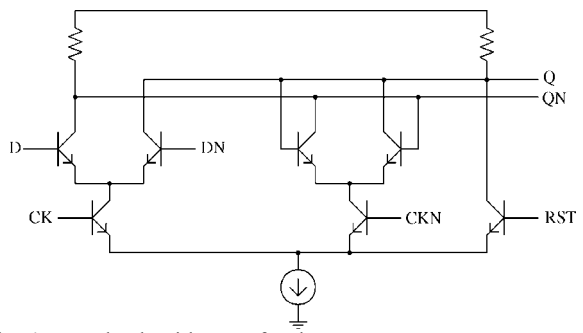

Fig. 4. D-latch with reset for the PFD.

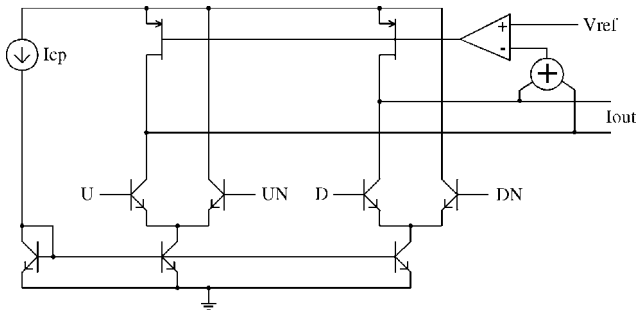

Fig. 5. Differential charge pump.

E. D2SE Amplifier

The D2SE amplifier is used to generate the single-ended control voltage for the VCO with minimum degradation of the VCO phase noise. It has been designed with about 100 MHz bandwidth, not to degrade the loop phase margin; moreover, low noise, high CMRR and PSRR and rail-to-rail output have been targeted. As shown in Fig. 6, the amplifier consists of a high common-mode rejection low leakage unity-gain CMOS differential stage, followed by a 9.5 dB difference amplifier. The latter gain has been fixed as a trade-off between low noise requirements and the need to limit the voltage swing on the loop filter; a reference voltage Vref has been introduced to halve the required input swing: it is required to be a low noise source, and has been left as an input pin of the device.

The operational amplifier features a folded architecture, using npn BJT and PMOS devices in cascode configuration, to enhance the bandwidth and optimize PSRR. A 3.3 V output stage has been used to maximize the swing at the interface with the VCO, and so the tuning range. Simulations have shown a closed loop bandwidth of 145 MHz, a CMRR of about 45 dB, a PSRR in excess of 40 dB and an output noise of 31 nV/√Hz.

IV. Technological Details and Measurements

The CMU has been integrated in STMicroelectronics BiCMOS7 technology [16], that is a SiGe HBT/CMOS technology suitable for RF system-on-chip applications.

The technology features high-frequency SiGe bipolar devices (f_T>65 GHz, β=100, BV_{CEO}=2.6 V, V_A>50 V) together with a 0.25 μm CMOS and a large set of passive components (resistors, MIM and MOS capacitors, varactors and spiral inductors). Five metal layers are provided for interconnections, with the top level

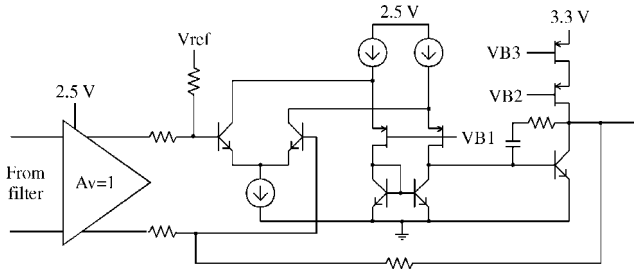

Fig. 6. D2SE amplifier.

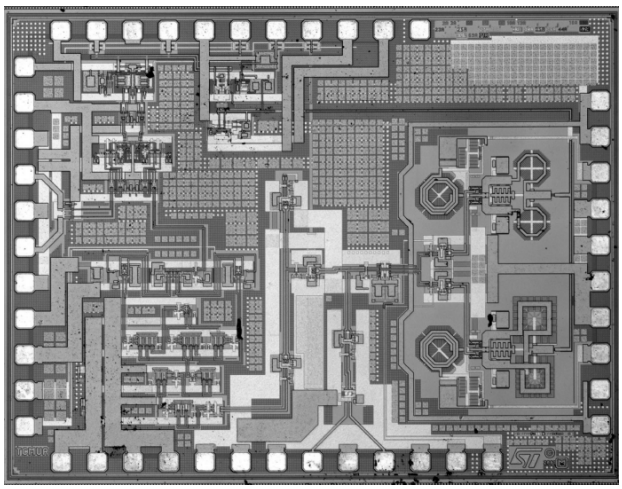

Fig. 7. Die micrograph.

optimized for the implementation of high-Q inductors.

Two power supplies have been used: 3.3 V for VCO and CML design (PFD, divider), and 2.5 V for CMOS analog design (PD, charge pump, D2SE); separate power supplies have been used to minimize high frequency coupling between critical blocks. Moreover, coupling has been minimized by using local bias generators for the various circuits, and a metal guard ring has been added around the VCOs to optimize phase noise performance by minimizing coupling with adjacent circuits. Attention has been paid to design a symmetrical layout so to exploit the advantages of differential signaling.

Fig. 7 shows a microphotograph of the chip, whose die size is 1.95x2.55 mm^2. The IC has been mounted bare die on a Arlon PCB for testing, together with the external loop filter, supply decoupling networks and dip switches for VCO and division ratio selection. An overall 150 mA current consumption from 3.3 V and 2.5 V supplies has been measured, for a total 480 mW power dissipation.

Measurements have been performed at 9.953 GHz using the Hewlett-Packard HP 70820 transition analyzer, and the output jitter is 80 mUIpp when measured with the bandpass filter specified in [2]. VCO phase noise has also been measured, resulting in –125 dBc/Hz at 10 MHz offset.

V. Conclusion

A fully monolithic 10 Gb/s Clock Multiplier Unit (CMU) IC featuring multistandard compliance with SDH/SONET and 10 GbE specifications has been succesfully implemented in a production level SiGe BiCMOS technology.

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