A 75 GHz Current Mode Logic Static Frequency Divider Realized in a Commercially Available InP Process

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***Abstract* — This work presents the fastest Current Mode Logic static frequency divider to date. The circuit is fabricated in a commercially available InP process. Microwave techniques are used to achieve speeds of 75 GHz without resort to emitter followers. Interconnect design is stressed and the results of several variations are presented. Microstrip, inverted microstrip, peaking inductors and keep-alive currents have all been fabricated and compared.**

I. Introduction

Static frequency dividers have been used as a benchmark for the upper limit of digital performance for a given process. Typically, these record setting test circuits are built for speed at the expense of power, die area and device count. The fastest reported circuit comes from HRL and uses Stacked Emitter Coupled Logic ("E^2CL") design to break 100 GHz [1]; the second fastest is from the laboratory process at UCSB and uses Emitter Coupled Logic ("ECL") design to achieve 87 GHz [2]. The present work uses a commercially available process and runs at 75 GHz in Current Mode Logic ("CML").

Large Scale Integration in InP is still a challenge. At this time the largest reported circuit known to the authors using InP HBTs is approximately 5,000 transistors [3], and operates at 40 GHz. By investigating microwave techniques for maximizing CML circuits, it is hoped that more functionality can be squeezed from the same device count and power consumption. Scaling is discussed in the context of a Method of Time Constant analysis, as well as the use of peaking inductors to improve rise times. The work here can easily be used for OC-768, without the need for any ECL stages. This allows for the reduction of both transistor count and power consumption. These circuits are readily reconfigured to form flip-flops, and it is the intent of the authors to use these high-speed CML latches as part of MSI and LSI circuits in the future. The reduced device count should help compensate for the lower yields of InP processes.

Results from five versions are presented here. The baseline design uses a keep-alive current, small peaking inductors, and a microstrip architecture with a suspended ground plane. Three variations were then made from this circuit: one without the keep-alive current; one without the peaking inductors; and one identical to the first but with an inverted microstrip architecture (the ground plane is on top of the circuit). The final version was a scaled up version of the baseline, with inverted microstrip.

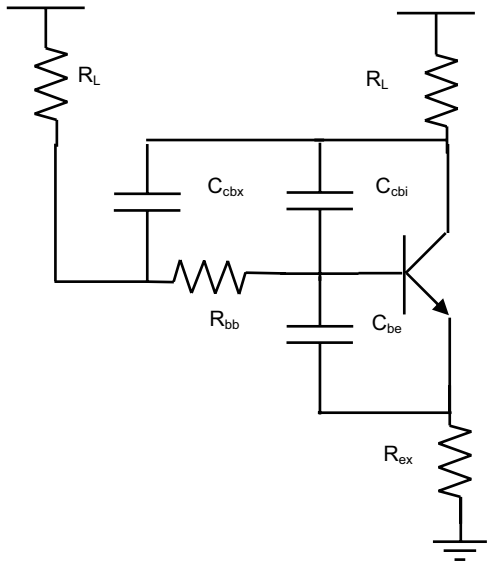

Fig. 1. Half-Circuit of CML Gate.

II. Circuit Analysis

The divider consists of two identical D-Latches, clocked 180 degrees out of phase. The output of the first latch is fed directly to the second latch, and the output of the second latch (which is also the output of the circuit) is fed back inverted to the input of the first latch.

A first order MOTC analysis of a CML gate is shown in Fig. 1 with the following simplifications: $\Delta V = R_L{*}I$; $A_V = -1$; $Gm = 1/R_L$; $C_{cbi} = C_{cbx} = \frac{1}{2} C_{cb}$.

$$
\begin{aligned}
a_1 &= C_{be}\left(R_{ex} \parallel \frac{1}{G_m} + R_{bb} + R_L\right) + C_{cbx}\left[R_L(1-A_V) + R_L\right] \\
&\quad + C_{cbi}\left[(R_L + R_{bb})(1-A_V) + R_L\right] \\
a_1 &\approx C_{je}\left(R_{ex} + R_{bb}\right) + \tau_f + C_{cb}R_{bb} + R_L(3C_{cb} + C_{je}) + \frac{1}{R_L}\tau_f(R_{ex} + R_{bb}) \\
a_1 &= K_1 + \frac{\Delta V}{AJ} A(3C_{cb0} + C_{jeo}) + \frac{AJ}{\Delta V}\tau_f\left(\frac{R_{exo} + R_{bbo}}{A}\right) \\
a_1 &= K_1 + \frac{\Delta V}{J} K_2 + \frac{J}{\Delta V} K_3 \qquad (1) \\
K_1 &= C_{jeo}\left(R_{exo} + R_{bbo}\right) + \tau_f + C_{cbo}R_{bbo} \\
K_2 &= (3C_{cb0} + C_{jeo}) \\
K_3 &= \tau_f(R_{exo} + R_{bbo})
\end{aligned}
$$

From (1) we can see that there exists an optimal current density for a given voltage swing. In practice, this current density exceeds the maximum allowable current density for the device. Therefore, all of the circuits were designed to run at the maximum current density. Furthermore, we can see that all of the RC products are independent of the area of the device, and depend only on the device characteristics (which are beyond the circuit designer's control). This is a direct result of maintaining the same logic swing. A larger device, running more current, will require a smaller load resistance, and vice versa. The parasitic resistances also scale inversely with the size, and the parasitic capacitances all scale directly with size. This being the case, it is desirable to make the device as small as possible to reduce the current (and power dissipation), and to minimize the length and effect of the interconnections. This was the principle used in the baseline version. However, the process rules may not allow the interconnections to scale as much as the device. In this case, top speed is obtained with the interconnects at the minimum feature size, and the devices scaled to provide maximum allowable current to the interconnects. This approach was used to create the fast design.

More detailed analysis of the complete circuit when level shifting emitter followers on the clock inputs (not shown here) are included, indicate that the emitter followers should be larger than the other transistors.

The keep-alive current is applied only to the tracking pair of each latch. The value of the current is set to one sixth of the value of the steering current [4]. This current prevents the tracking pair from completely switching off during the hold cycle of the latch. Since V_{be} has an exponential relationship to the current flowing through the transistors, less charging is necessary for C_{be} when the transistor switches. The net result is that the voltage swing across C_{be} is reduced, and the keep-alive current helps the track pair in switching. The drawback of the keep-alive current is its affect on the output. For half of the hold stage, the tracking pair is receiving the opposite signal as the hold pair. The keep-alive current is thus steered to the wrong collector resistor. The result is that the output of the circuit is reduced for half of the cycle. This is clearly seen in Fig. 7. It is interesting to note that applying a keep-alive current to the hold pair impairs performance, and the maximum speed of operation is reduced.

From the MOTC analysis we can see that an emitter follower would reduce the source resistance seen at the base of the switching transistor from R_L to $1/g_m$. Decoupling the source resistance from C_{be} gives an additional degree of freedom to the designer in scaling devices. This can be used to generate a significant improvement in rise times. Without emitter followers, peaking inductors in series with the collector resistors can be used to generate a similar improvement in rise times. Shunt peaking is a well understood technique [5], and its effect can be characterized with a factor m:

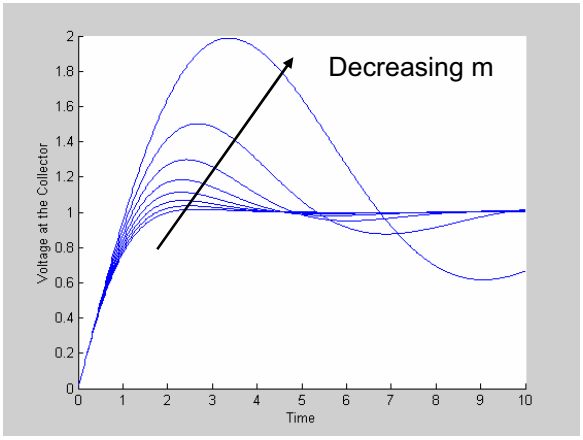

Fig. 2. Step response for decreasing m.

$$m = \frac{RC}{L/R} = \frac{R^2C}{L}$$
$$R\alpha\frac{1}{A};\ C\alpha A$$
$$\Rightarrow L\alpha\frac{1}{A} \qquad (2)$$

Here, R is the load resistance, and C is the collector-base capacitor. Assuming the logic swing and optimum current density are constant, the load resistance will scale inversely with emitter area, and the capacitance will scale directly with area. From Fig. 2, we can see that for a given peaking behavior (m value) the inductance scales inversely with emitter area. Given this relationship and the physical difficulty in laying out an inductor in a small area we can see that we want a larger emitter area for a smaller optimum inductance. This is utilized in the fast divider.

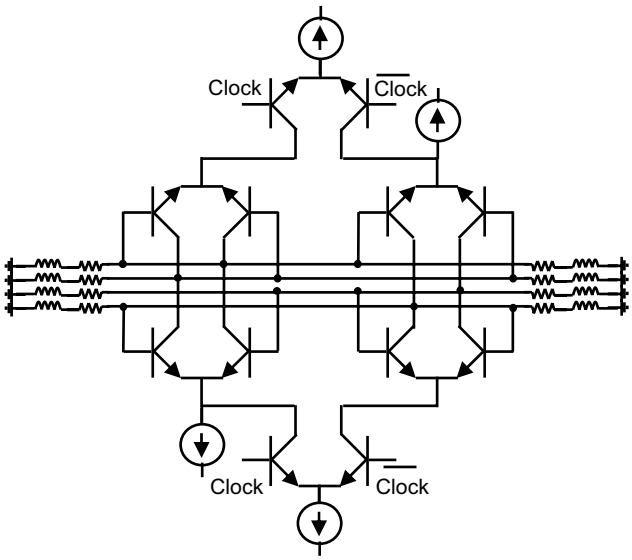

Fig. 3. Basic layout for divider circuit.

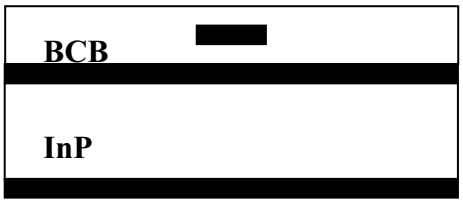

Fig. 4. Suspended Microstrip

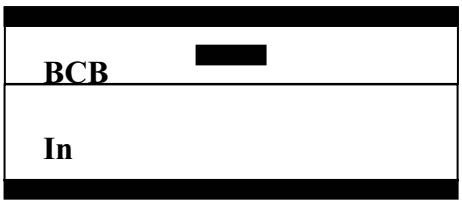

Fig. 5. Inverted Microstrip

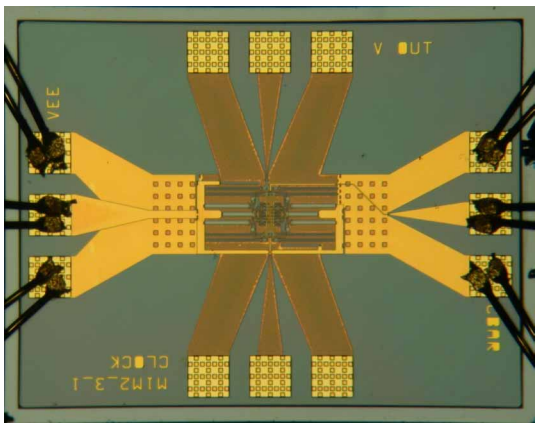

Fig. 6. Picture of Baseline circuit

III. Circuit Implementation

The basic circuit topology is shown in Fig. 3. Symmetry is observed wherever possible, and the collectors are doubly terminated. The circuits are designed for an internal swing of 300 mV. The clock is fed through level shifting emitter followers to the latches. The output is taken single ended without a buffer. The outputs of the baseline version and its variations are taken with an on-chip 450 Ohm resistor in series with the oscilloscope, all in parallel with the collector's load resistor. This reduces the loading on the circuit and results in a waveform at the oscilloscope whose amplitude is one tenth of the internal swing. The fast divider uses inverted microstrip (Fig. 5); has an open collector utilizing the 50 Ohm oscilloscope as a load resistor; and delivers full swing to the oscilloscope.

Current sources are realized by pull-down resistors. Peaking inductors are realized as transmission lines that are laid out parallel to the pull down resistors (thus contributing little to the overall size of the circuit).

The wiring environment is microstrip between the two latches where the interconnections are the most dense. Outside of this center area, the wiring is coplanar. Simulations using the backplane as ground for the microstrip failed at 20 GHz, due to ringing on the signal lines. Therefore, one of the metal layers is used for ground. The suspended microstrip uses the first metal layer for ground, shielding the interconnects from the back plane, Fig. 4. The inverted microstrip uses the third metal layer for ground, Fig. 5. Both configurations provide for a very close ground plane, reducing the cross talk, and allowing for tight layout. Using the inverted microstrip also allows for an even more tightly packed circuit since it reduces the number of vias required. For this work, the last property was not exploited, and the two versions employ exactly the same footprint. A picture of the baseline circuit is shown in Fig. 6.

IV. Measurements and Results

Measurements were performed from 3 GHz to 75 GHz. For frequencies up to 40 GHz, the clock was applied directly from a frequency synthesizer. Without a limiting amplifier on the input, the dividers were driven with a sine wave. This results in a lower limit on the operating range of the circuit. Fig. 7 shows output at 10 GHz with -1 dBm input power, confirming the static nature of the frequency divider.

For frequencies between 50 GHz and 75 GHz an active frequency tripler was used. The output passed through a V-band waveguide to a waveguide-coupled micro-coaxial probe. The divided output for a 75 GHz input clock is shown in Fig. 8. There is significant sub-harmonic distortion. Fig. 9 shows the output of the frequency tripler at 50 GHz. The same subharmonic distortion is present in the clock, though to a lesser degree. We were unable to measure the output of the tripler directly at 75 GHz to see the level of distortion present, although we believe this to be a source of the output modulation.

Table 1 shows the summary of the results of the various versions of the circuit, with their maximum speeds of operation, and their current. All circuits use –5.0V supply. A sensitivity plot was made for both the fast circuit, and a typical baseline circuit (maximum speed 62 GHz). Both of these plots are in Fig. 10.

TABLE I
Summary of Results

Design	Maximum Speed	Current
Baseline	67 GHz	28.6 mA
Without keep-alive	62 GHz	27.6 mA
Without Inductors	65 GHz	30.5 mA
Inverted Microstrip	68 GHz	30.4 mA
Fast	75 GHz	92.7 mA

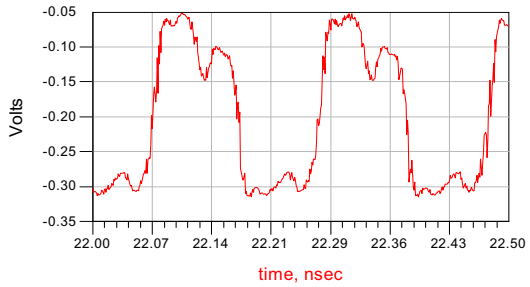

Fig. 7. Output of fast divider with 10 GHz clock in.

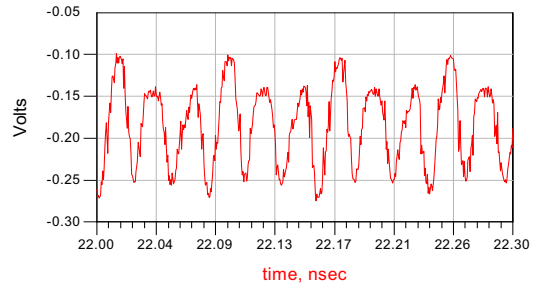

Fig. 8. Output of fast divider with 75 GHz Clock in

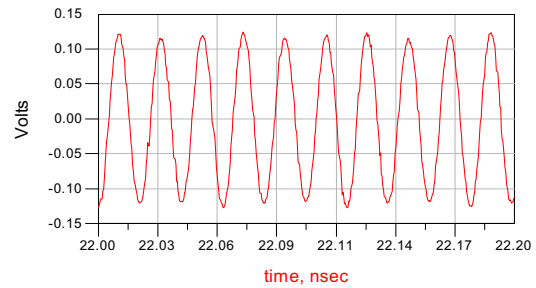

Fig. 9. Clock from frequency tripler at 50 GHz out

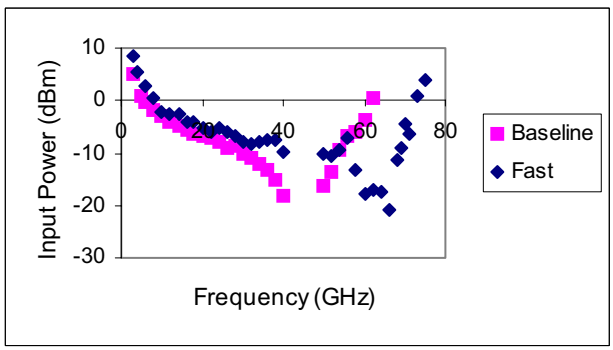

Fig. 10. Sensitivity plot for baseline and fast dividers

V. Conclusion

This paper has reported the fastest CML divider known to the authors. Comparison of microstrip and inverted microstrip structures shows that the two have similar performance. The inverted microstrip architecture shows potential for reduced interconnection length (due to the reduced number of vias) and improved speed. The keep-alive current is a significant improvement for a relatively small increase in current. The shunt stub inductors provide a smaller improvement in the 60 GHz region, but they do not cost anything in power. At higher frequencies, these will provide greater improvements for the same length transmission line stub. These circuits are clearly capable for OC-768 applications, but are unlikely to be useful at 80 GHz region.

Acknowledgement

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