A Monolithically Integrated InP-Based HBT and p-i-n Photodiode Using New Stack-Shared Layer Scheme

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Abstract — **New stack-shared layer scheme has been developed to integrate monolithically InP-based heterojunction bipolar transistor (HBT) and p-i-n photodiode. In this layer scheme, a p^+- and intrinsic InGaAs layers for a photodiode were stacked on n^+-InP emitter layer, which is shared as both emitter contact layer for an HBT and n-type contact layer for a photodiode. The fabricated HBTs demonstrated excellent high-speed characteristics of f_T = 108 GHz and f_{max} = 300 GHz. The photodiode, formed with an undoped 4300 Å-thick InGaAs as an absorption layer, exhibited a dark current of 6 nA under 5 V reverse bias, with a responsivity of 0.3 A/W at 1.55 μm optical radiation. A 3-dB bandwidth of the photodiodes with diameters smaller than 25 μm was over 20 GHz. High-frequency performances of both devices were observed due to the advantages of the stack-shared layer scheme, characterized by independent optimization of the device layer structure and moderate nonplanarity.**

I. Introduction

Monolithically integrated photoreceivers based on InP/InGaAs material systems have been intensively investigated because of their advantages for high-speed operation and material compatibility of transistors and photodiodes for long-wavelength (1.3–1.55 μm) optical communication. The key issue in the photoreceiver technology is the development of a photodiode, which is compatible with the already existing HBT technology. In general, there are two design approaches to the monolithic integration of transistors and photodiodes with different layer structures. In the first approach, either a stacked layer scheme [1] or regrowth of one of the device structures [2] is used to fabricate the devices on a same substrate. This approach advantages independent optimization of the two different devices, while growth complexity, low yield, and high nonplanarity have been emerged as major disadvantages. The second approach is to use the shared layer structure for both devices [3]–[5]. Compared to the first approach, this layer design provides simpler fabrication and higher yield, but with the disadvantages such as inevitable compromise of the individual device performance. In this work, new stack-shared layer scheme, which one layer is shared for both devices and the others are stacked on an HBT layer, is used to the monolithic integration of InP-based HBT and p-i-n photodiode.

In this letter, the device structure design using stack-shared layer scheme is investigated in detail. The device fabrication technology developed for the monolithic integration and the measured performance of the devices are also discussed.

II. Stack-Shared Layer Scheme

The device layer structure employing stack-shared layer scheme was grown by MBE using Si and C for n- and p-type dopants, respectively. It consists of typical base-collector layers on a semi-insulating InP substrate, followed by a 600-Å n-InP emitter layer, an 1000-Å n^+-InP emitter layer, a 4300-Å InGaAs absorption layer, an 1000-Å p^+-InGaAs contact layer, and undoped 800-Å InP and 100-Å InGaAs transfer layers. The parameters of the layers are summarized in Table I. In this stack-shared layer structure, the p^+- and intrinsic InGaAs layers for the p-i-n photodiode were stacked on the heavily doped InP (2×10^{19} cm^{-3}) emitter layer, which is used as both emitter contact layer for an HBT and n-type contact layer for a photodiode. The two upper InGaAs/InP layers are used to transfer an emitter stripe to the p^+-InGaAs contact layer in the photolithography process, therefore, producing a crystallographically defined emitter contact (CDC) [6] for self-aligning an emitter/base contact of an HBT using anisotropic wet etching characteristics of InGaAs [7].

A schematic cross sectional view of InP/InGaAs HBT and stack-shared p-i-n photodiode is shown in Fig. 1. In this layer structure, the thin InGaAs absorption and shared n^+-InP emitter layers provide more moderate nonplanarity compared to the stack layer structure, producing further facilitation of device fabrication. With respect to the photodiode performance, the lowest possible collector doping level should be used to reduce the dark current [8]. In the shared layer scheme, this minimum doping level is, however, limited under HBT performance considerations because at low doping base push-out occurs even at a low collector current density and then a phenomenon known as the Kirk effect results in degrading seriously high-frequency performances. In the shared structure, the collector thickness also influences the performance of each device. The collector should be thinner to enhance high-speed operation of the photodiode. However, thinner collector layer causes higher base-collector capacitance, degrading a maximum oscillation frequency (f_{max}). Therefore, the consideration of the effect of collector thickness and collector doping on transistor and photodiode cannot be optimized simultaneously in the shared layer structure.

Table I. Device layer structure of InP/InGaAs HBT and stack-shared p-i-n photodiode.

Layer	Material	Doping (cm^{-3})	Thickness (nm)
Transfer	u-InGaAs	undoped	10
	u-InP	undoped	80
Dummy emitter	p^+-InGaAs	4×10^{19}	100
	i-InGaAs	2×10^{15}	430
Emitter	n^+-InP	2×10^{19}	100
	n-InP	4×10^{17}	60
Spacer	u-InGaAs	undoped	5
Base	p^+-InGaAs	4×10^{19}	45
Collector	n-InGaAs	2×10^{16}	600
Etch-stop	n^+-InP	2×10^{19}	10
Subcollector	n^+-InGaAs	2×10^{19}	400

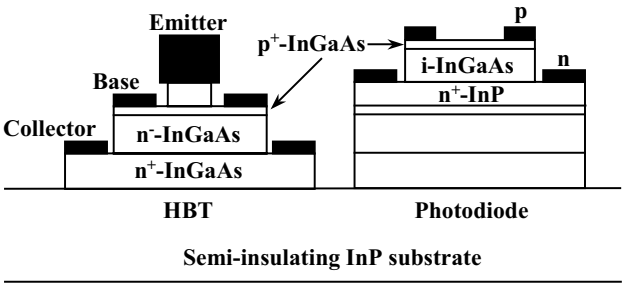

Fig. 1. Schematic cross-section view of InP/InGaAs HBT and surface-illuminated InGaAs/InP p-i-n photodiode using stack-shared layer scheme.

However, in the stack-shared structure, the minimum doped 4300-Å absorption layer (2×10^{15} cm^{-3}) is completely separated from the 6000-Å collector layer with a doping level of 2×10^{16} cm^{-3}, indicating that it is possible to optimize independently both devices.

The bandwidth of the photodiode is limited by both the carrier transit time and the RC time constant. Carrier transit time can be decreased by thinning the absorption layer, whereas the junction capacitance is reduced by thickening the absorption layer or decreasing device area. Fig. 2 shows the dependence of the calculated bandwidth in the photodiode on intrinsic absorption layer thickness. For a given device area, there exists an optimum absorption layer thickness in order to satisfy both requirements. Therefore, the absorption layer thickness is designed to be 4300-Å to obtain the maximum bandwidth in a 15 μm-diameter device.

III. Monolithic Integration Technology

Crystallographically defined emitter contact (CDC) technology using anisotropic wet etching characteristics of the InGaAs layer, which serves as a p-type layer and an intrinsic absorption layer in the photodiode, is employed for self-alignment in the InP/InGaAs HBTs [6]. Generally, a heavily doped InGaAs layer is widely used to obtain a low ohmic contact resistance. However, a heavily doped InP emitter layer is used as an emitter contact layer to obtain a consistent crystallographically defined emitter contact using high etching selectivity between the InP emitter layer and its upper InGaAs layer.

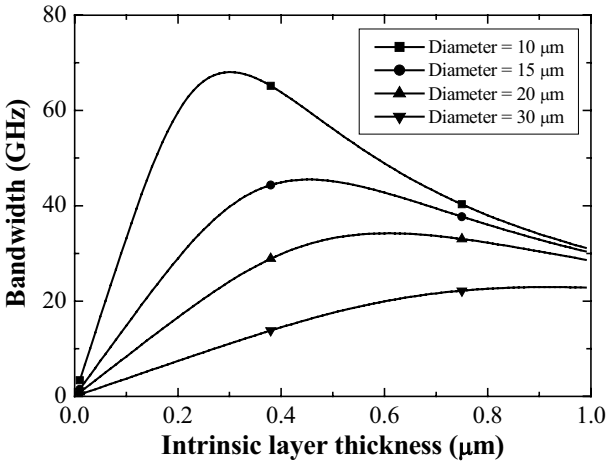

Fig. 2. Calculated bandwidth of a p-i-n photodiode as a function of an intrinsic layer thickness.

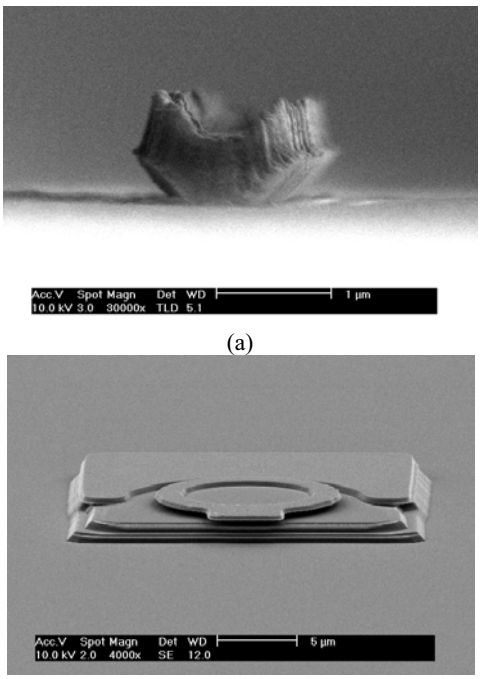

Fig. 3. SEM photographs of (a) the emitter contact using CDC technology and (b) the p-i-n photodiode.

Transmission line model (TLM) measurements indicated the specific contact resistance of 3.52×10^{-7} $\Omega \cdot cm^2$ for n^+-InP emitter layer, comparable to that of InGaAs used as a contact layer [9]–[10].

A fabrication process for monolithic integration starts with the formation of p-type contact (Pt/Ti/Pt/Au) for the photodiode on the upper p^+-InGaAs layer. An n-type contact (Ti/Pt/Au) for the photodiode is formed on the heavily doped InP emitter layer and at the same time an emitter metal (Ti/Pt/Au) of the HBT using CDC technology is deposited on the same layer. Then, mesa etching for definition of absorption area and emitter mesa etching are performed sequentially. These processing steps complete a photodiode structure. Its device area is covered with a photoresist while the fabrication process for an HBT has been in progress. Next, a self-aligned base contact (Pt/Ti/Pt/Au) is evaporated without the electrical short-circuit due to the shape of the emitter

contact (Fig. 3 (a)). Subsequent processing steps are the same as those in the previously published report [6], [11]. A polyimide is used for both device passivation and antireflection coating. Fig. 3 shows the scanning electron micrograph (SEM) photographs of the emitter contact employing CDC technology and the p-i-n photodiode. As shown in Fig. 3 (a), the shape of the emitter contact is effective in producing the consistent alignment of the emitter and base contacts. At the photodiode mesa etching, selective sidewall etching was performed to achieve a mushroom type mesa structure, as shown in Fig. 3 (b), which helps to reduce the junction capacitance of the photodiode.

IV. Results and Discussions

The device performances on transistor and photodiode are investigated and discussed to evaluate the stack-shared layer scheme. First, DC and RF measurements of the fabricated HBTs are performed. The common-emitter characteristics of a fabricated 1.4 × 10 μm^2 emitter device are shown in Fig. 4. The offset voltage ($V_{CE,\ offset}$) was measured to be as low as 0.15 V. The knee voltage was approximately 0.5 V up to a collector current density (J_C) of 1 × 10^5 A/cm^2. These measurement values verify that n$^+$-InP emitter layer used as an emitter contact layer does not result in degraded DC characteristics of the fabricated HBT device. The DC current gain (h_{FE}) of 35 was obtained from the fabricated device with the ideality factors of n_C = 1.18 and n_B = 1.48. The collector-emitter breakdown voltage (BV_{CEO}) was 8.9 V.

Fig. 5 shows the frequency dependence of current gain ($|h_{21}|^2$), maximum stable gain/maximum available gain (*MSG/MAG*), and unilateral power gain (U) for a fabricated 1 × **2**0 μm^2 emitter device. The maximum f_T and f_{max} in this device were estimated to be 108 GHz and 300 GHz, respectively, by extrapolating the measured $|h_{21}|^2$ and U with a 20 dB/decade falloff slope. These excellent high-frequency characteristics were obtained due to the very low product of reduced R_B and C_{BC}, resulting from the optimized base mesa etching and CDC technologies.

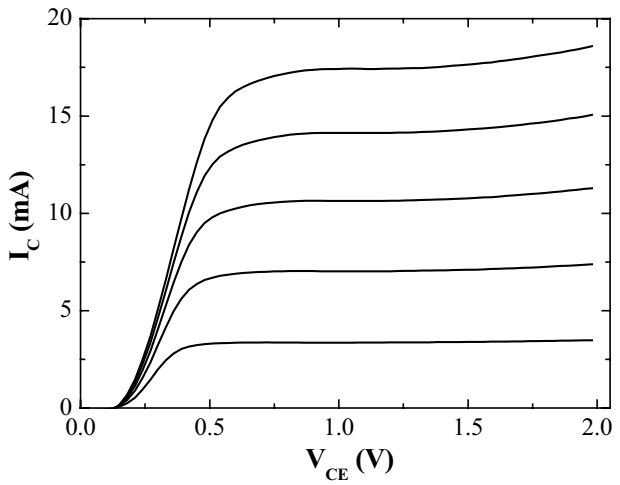

Fig. 4. Common-emitter I_C-V_{CE} characteristics of a 1.4 × 10 μm^2 InP/InGaAs HBT.

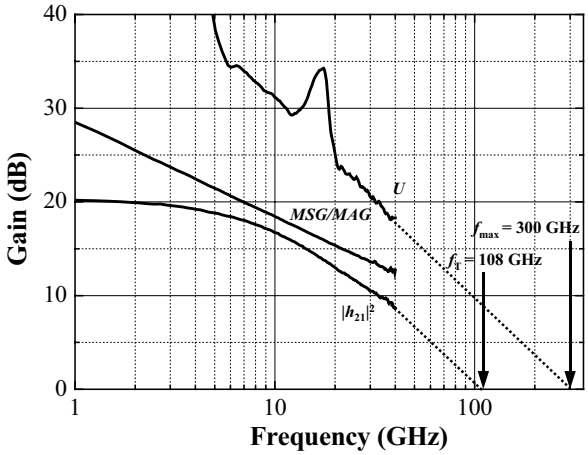

Fig. 5. Dependence of $|h_{21}|^2$, *MSG/MAG* and U on frequency of the fabricated HBT with a 1 × 20 μm^2 emitter size at bias condition of V_{CE} = 1.5 V and I_C = 17 mA.

In order to evaluate the effects of integration on the performance of the photodiode, the stack-shared InGaAs/InP p-i-n photodiodes with various mesa areas were fabricated. Photoresponse measurements were carried out in the 1550 nm using a laser source. The optical output of the laser was coupled to a single mode fiber. Fig. 6 shows the photoresponse characteristics of a 20 μm-diameter p-i-n photodiode in the dark and with 1.55 μm optical illumination. The fabricated photodiode with the 4300 Å-thick intrinsic InGaAs exhibited a dark current of 6 nA under 5 V reverse bias, with a responsivity of 0.3 A/W, corresponding to an external quantum efficiency of 24 %. The incident optical power was stepped down from 1.1 mW by four-fold for each curve. The constant spacing between curves shows the linearity of the photodiodes at these optical power levels, as seen in Fig. 6.

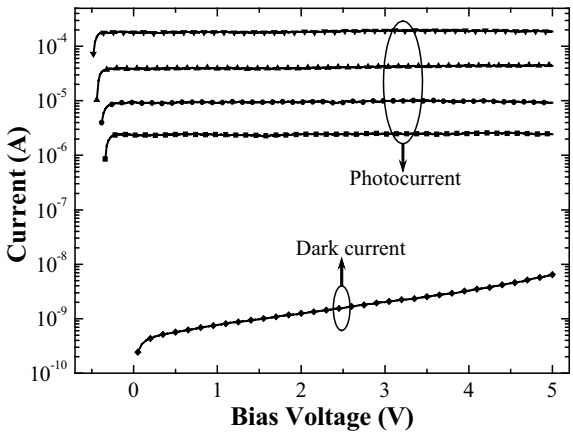

Fig. 6. Photoresponse characteristics of the fabricated p-i-n photodiode in the dark and with 1.55 μm illumination.

The frequency response of these photodiodes was characterized using an Agilent 8703B lightwave component analyzer from 1 GHz to 20 GHz. As shown in Fig. 7, a 3-dB bandwidth was measured to be 5.6 GHz and 13.2 GHz for 30 μm and 50 μm devices, respectively, at a reverse bias of 2 V. The measurement results of the

25 μm-diameter device exhibited the bandwidth in excess of 20 GHz, which is limit of the measurement equipment. As a diameter of the devices is smaller, the bandwidth of the photodiode increases gradually. The reason of the enhancement of frequency response is that the junction capacitance is decreased as the dimension of the devices is reduced. The RC time constant limited bandwidth of the 20 μm device, which obtained almost flat response to 20 GHz, is calculated to be 34.4 GHz. On the other hand, its calculated transit time limited bandwidth is estimated to be as high as 69.3 GHz due to thin intrinsic InGaAs layer [12]. Considering both limiting factors, the 3-dB bandwidth is calculated to be 30.8 GHz. Therefore, the frequency response of the photodiode with diameters larger than 20 μm is dominated by RC time constant limited effect, which is mainly affected by the junction capacitance. High-frequency performances of the p-i-n photodiode were observed due to the advantages of the stack-shared layer scheme, characterized by independent optimization of the device layer structure.

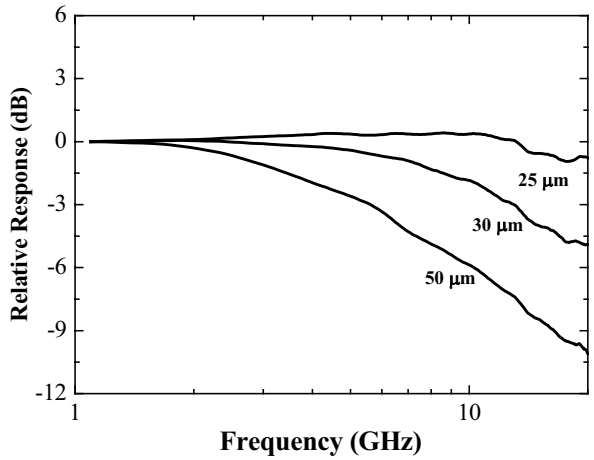

Fig. 7. Frequency response of the stack-shared p-i-n photodiode with various diameters.

V. Conclusion

The monolithically integrated InP-based HBT and p-i-n photodiode using stack-shared layer scheme have been successfully demonstrated. In this layer scheme, a p^+- and intrinsic InGaAs layers for a photodiode were stacked on n^+-InP emitter layer, which is shared as both emitter contact layer for an HBT and n-type contact layer for a photodiode. The fabricated HBTs demonstrated excellent high-speed characteristics of f_T = 108 GHz and f_{max} = 300 GHz. The photodiode exhibited a dark current of 6 nA under 5 V reverse bias, with a responsivity of 0.3 A/W at 1.55 μm optical radiation. The 3-dB bandwidth of the photodiodes with diameters smaller than 25 μm was over 20 GHz. Newly developed layer design is promising for fabrication of a photoreceiver by an independent device optimization with further facilitation of device fabrication due to moderate nonplanarity.

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