Physics-Based Device Simulation of Lag and Power Compression in GaAs FETs

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Abstract — **Two-dimensional transient simulation of GaAs FETs are performed in which substrate traps, surface states and impact ionization of carriers are considered. The mechanisms of lag phenomena and so-called power compression are discussed. It is shown that the drain-lag occurs mainly due to substrate traps, and the gate-lag mainly by surface states. Obtained quasi-pulsed *I-V* curves clearly indicate that the power compression can occur both due to substrate traps and due to surface states. Effects of the impact ionization on these phenomena are also discussed.**

I. INTRODUCTION

Compound semiconductor FETs, such as GaAs MESFETs, GaAs-based HEMTs, and GaN-based FETs, are very important devices for microwave power devices and ICs that are now receiving great interest, particularly for mobile communication applications. In the high power microwave devices, stable high-voltage and high-frequency operation is required. In the compound semiconductor FETs, however, slow current transients are often observed even if the gate or drain voltage is changed abruptly [1],[2]. This is called gate-lag or drain-lag. These slow current transients indicate that the DC *I-V* curves and the AC *I-V* curves become quite different, resulting in lower AC power available than that expected from the DC operation [3],[4]. This is called power compression. These phenomena are serious problems, but their detailed mechanisms are not necessarily well understood. Although there are many experimental works reported on these phenomena, few theoretical works have been reported.

Therefore, in this work, we have made physics-based transient simulations in which substrate traps, surface states and impact ionization of carriers are considered, and studied how the lag phenomena are influenced by these factors. In addition, we have derived quasi-pulsed *I-V* curves from the transient characteristics, and discussed how they differ from the DC *I-V* curves. As a result, it has been clearly shown that the power compression can occur both due to substrate traps and due to surface states.

II. PHYSICAL MODEL

Fig.1 shows a modeled GaAs MESFET analyzed in this study. As a substrate, we consider undoped semi-insulating GaAs where deep donors "EL2" (N_{EL2}) compensate shallow acceptors (N_{Ai}) [5]. The substrate-trap effects may be similar in GaAs-based HEMTs (PHEMTs) because the same type of substrate is used [3].
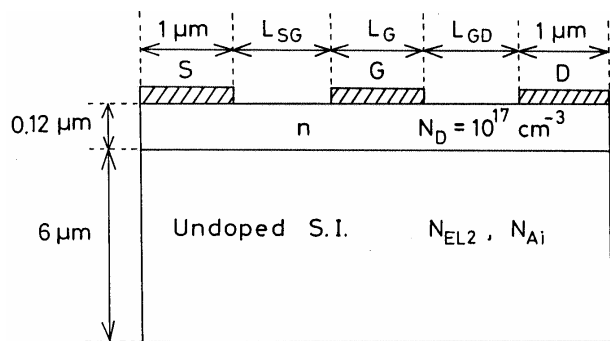

Fig.1. Device structure simulated in this study.

The structure in Fig.1 is similar to GaN MESFETs where a semi-insulating buffer layer with traps exists under an active layer [2].

The surface states are considered on the planes between the source and the gate and on the planes between the gate and the drain. As a surface-state model, we adopt Spicer's unified defect model [6], and assume that the surface states consist of a pair of a deep donor and a deep acceptor. The surface states are assumed to distribute uniformly within 5 Å from the surface, and their densities are typically set to 10^{13} cm^{-2} (2×10^{20} cm^{-3}). As for their energy levels, the following case based on experiments is considered as in previous works [7],[8]: $E_{SD} = 0.87$ eV, $E_{SA} = 0.7$ eV [9],[10], where E_{SD} is energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is energy difference between the deep acceptor's energy level and the top of valence band.

Basic equations to be solved are Poisson's equation, continuity equations for electrons and holes and rate equations for the deep levels [7],[8]. They are expressed as follows.

1) Poisson's equation

$$\nabla^2 \psi = -\frac{q}{\varepsilon}(p - n + N_D - N_A + N_{EL2}^+ + N_{SD}^+ - N_{SA}^-) \quad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \bullet J_n + G - (R_{n,EL2} + R_{n,SD} + R_{n,SA}) \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \bullet J_p + G - (R_{p,EL2} + R_{p,SD} + R_{p,SA}) \quad (3)$$

where

$$R_{n,EL2} = C_{n,EL2}N_{EL2}^{+}n - e_{n,EL2}(N_{EL2} - N_{EL2}^{+}) \quad (4)$$

$$R_{n,SD} = C_{n,SD}N_{SD}^{+}n - e_{n,SD}(N_{SD} - N_{SD}^{+}) \quad (5)$$

$$R_{n,SA} = C_{n,SA}(N_{SA} - N_{SA}^{-})n - e_{n,SA}N_{SA}^{-} \quad (6)$$

$$R_{p,EL2} = C_{p,EL2}(N_{EL2} - N_{EL2}^{+})p - e_{p,EL2}N_{EL2}^{+} \quad (7)$$

$$R_{p,SD} = C_{p,SD}(N_{SD} - N_{SD}^{+})p - e_{p,SD}N_{SD}^{+} \quad (8)$$

$$R_{p,SA} = C_{p,SA}N_{SA}^{-}p - e_{p,SA}(N_{SA} - N_{SA}^{-}) \quad (9)$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{EL2} - N_{EL2}^{+}) = R_{n,EL2} - R_{p,EL2} \quad (10)$$

$$\frac{\partial}{\partial t}(N_{SD} - N_{SD}^{+}) = R_{n,SD} - R_{p,SD} \quad (11)$$

$$\frac{\partial}{\partial t}N_{SA}^{-} = R_{n,SA} - R_{p,SA} \quad (12)$$

where N_{EL2}^{+}, N_{SD}^{+} and N_{SA}^{-} represent ionized densities of substrate trap:EL2, surface deep donors and surface deep acceptors, respectively. C_n and C_p are the electron and hole capture coefficients of the deep levels, respectively, e_n and e_p are the electron and hole emission rates of the deep levels, respectively, and the subscript (EL2, SD, SA) represents the corresponding deep level. G represents a carrier generation rate by impact ionization, and is expressed as

$$G = (\alpha_n |J_n| + \alpha_p |J_p|)/q \quad (13)$$

where α_n and α_p are ionization rates for electrons and holes, respectively, and are given by [11]

$$\alpha_n = A_n \exp\{-(B_n/|E|)^{1.6}\} \quad (14)$$

$$\alpha_p = A_p \exp\{-(B_p/|E|)^{1.75}\} \quad (15)$$

where E is the electric field. $A_n = 2.994 \times 10^5$ cm^{-1}, $A_p = 2.215 \times 10^5$ cm^{-1}, $B_n = 6.848 \times 10^5$ V/cm and $B_p = 6.570 \times 10^5$ V/cm [11].

The above equations are put into discrete forms and are solved numerically. We have calculated the turn-on characteristics when the gate voltage V_G and the drain voltage V_D are both changed abruptly.

III. Effects Of Substrate Traps

Fig.2 shows calculated turn-on characteristics of a GaAs MESFET on the semi-insulating substrate ($N_{Ai} = 10^{16}$ cm^{-3}) when V_G is changed from the threshold voltage V_{th} to 0.4 V. (The surface states are not included.) Here, the off-state drain voltage V_{Doff} is 10 V, and the parameter is the on-state drain voltage V_{Don}. The solid lines are calculated by considering impact ionization of carriers, and the dashed lines by neglecting it.

When V_{Don} is 10 V, that is, the drain voltage is not changed, the drain current reaches the steady-state value soon, indicating little gate-lag in this case. When V_{Don} is
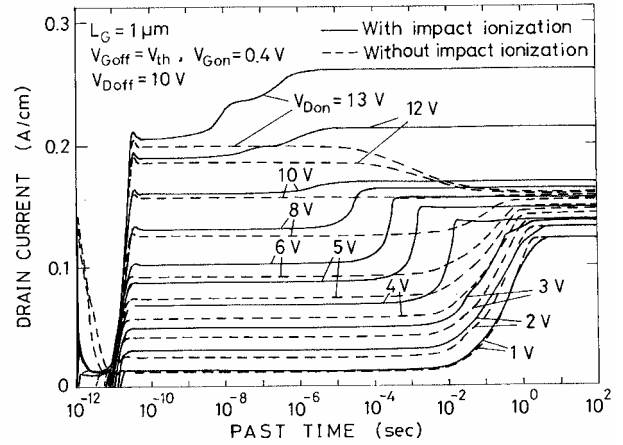

Fig.2. Calculated turn-on characteristics of GaAs MESFET on the semi-insulating substrate ($N_{Ai} = 10^{16}$ cm^{-3}), with on-state drain voltage V_{Don} as a parameter. $V_{Doff} = 10$ V. $V_{Goff} = V_{th}$ and $V_{Gon} = 0.4$ V.
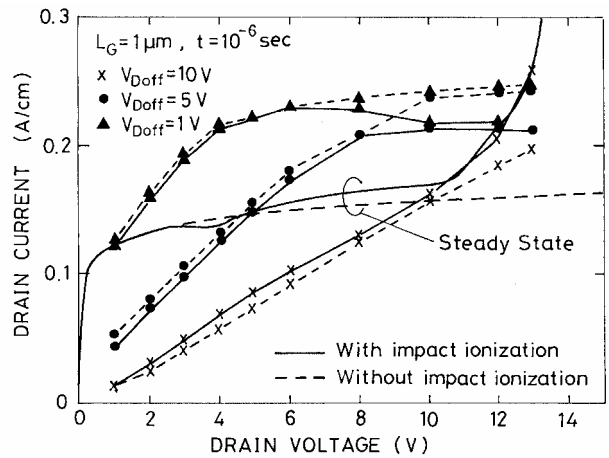

Fig.3. Drain currents at $t = 10^{-6}$ sec after the gate voltage is switched-on. (x): $V_{Doff} = 10$ V (corresponds to Fig.2), (●): $V_{Doff} = 5$ V, (▲): $V_{Doff} = 1$ V.

lower than 10 V, the drain currents remain at low values for some periods, and begin to increase slowly, showing large drain-lag. Without impact ionization, the drain currents begin to increase due to electron emission from the substrate trap: EL2. With impact ionization, the response is faster particularly at high voltages. Without impact ionization and for V_{Don} higher than 10 V, the drain currents overshoot, showing other type of drain-lag. The detail on these points will be described later.

Fig.3 shows calculated drain current versus drain voltage curves. In the steady state or DC state, so-called kink arises around 4 V, and a clear increase in drain current occurs beyond 10 V. In this figure, we plot by point (x) the drain current at $t = 10^{-6}$ sec after V_G is switched-on. This is obtained from Fig.2, and this curve corresponds to a quasi-pulsed I-V curve. At low voltages, the drain currents in the pulsed I-V curve are much lower than those for DC state. This indicates that so-called power compression occurs due to substrate traps. In this figure, we also plot other quasi-pulsed I-V curves for the cases of $V_{Doff} = 5$ V and 1 V by (●) and (▲), respectively. It is seen that when V_D is raised, the drain currents become temporarily higher than those for DC state. This
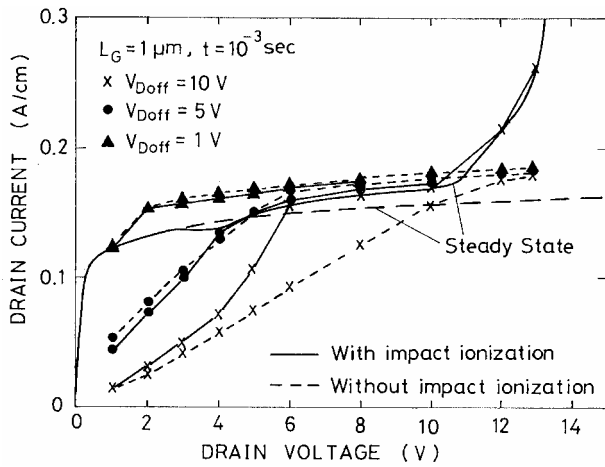
Fig.4. Drain currents at $t = 10^{-3}$ sec after the gate voltage is switched-on. (x): $V_{Doff} = 10$ V (corresponds to Fig.2), (●): $V_{Doff} = 5$ V, (▲): $V_{Doff} = 1$ V.

Fig.5. Calculated turn-on characteristics of GaAs MESFET with surface-state densities of 10^{13} cm^{-2}, with on-state drain voltage V_{Don} as a parameter. $V_{Doff} = 5$ V. $V_{Goff} = V_{th}$.

is because when V_D is raised, electrons are injected into the substrate, and the substrate trap: EL2 needs certain time to capture these electrons.

Fig.4 shows similar pulsed I-V curves, where we plot the drain currents at $t = 10^{-3}$ sec after V_G is switched-on. The power compression is still observed at low voltages, but the drain currents become equal to the DC values at relatively high voltage region, where impact ionization of carriers becomes important. This is understood that generated holes by impact ionization are injected into the substrate and are captured by EL2, playing the same electrical role as electron emission from EL2. Therefore, the response is faster at high voltages.

IV. EFFECTS OF SURFACE STATES

Next, we describe effects of surface states on lag phenomena and pulsed I-V curves (or power compression). Fig.5 shows calculated turn-on characteristics of a GaAs MESFET with surface-state densities of 10^{13} cm^{-2}. The substrate is assumed perfectly insulating without traps. Here, V_{Goff} is equal to V_{th}, and V_{Doff} is 5 V. The parameter is V_{Don}. In general, the drain currents remain at low values for some periods, and begin to increase slowly, showing lag behavior. This is due to the slow response of surface states [12]. Although the drain-voltage dependence is seen, the gate-lag is regarded as predominant in this case. It is also seen that the lag is smaller when impact ionization of carriers is included. This is described in [8], and this tendency is consistent with experiments [13].

Fig.6 shows quasi-pulsed I-V curves, where we plot by point (○) the drain currents at $t = 10^{-3}$ sec after V_G is switched-on. In this figure, we also plot another quasi-pulsed I-V curve for the case of $V_{Doff} = 1$ V by (△). At all drain voltages, the drain currents in the pulsed I-V curves are much lower than those for DC state. This indicates that the power compression could also occur due to surface states, although the power compression or the gate-lag is smaller when impact ionization of carriers is included.
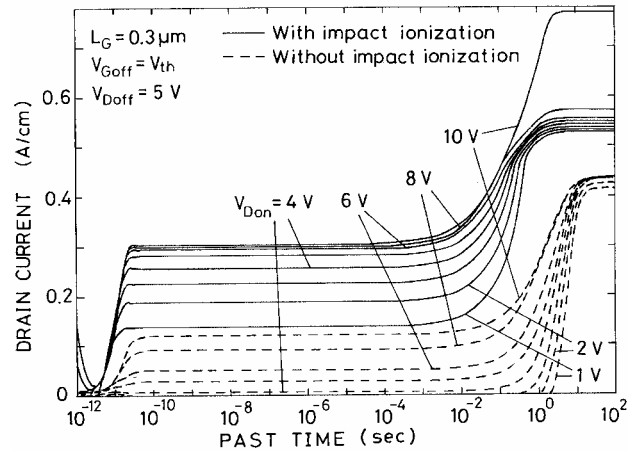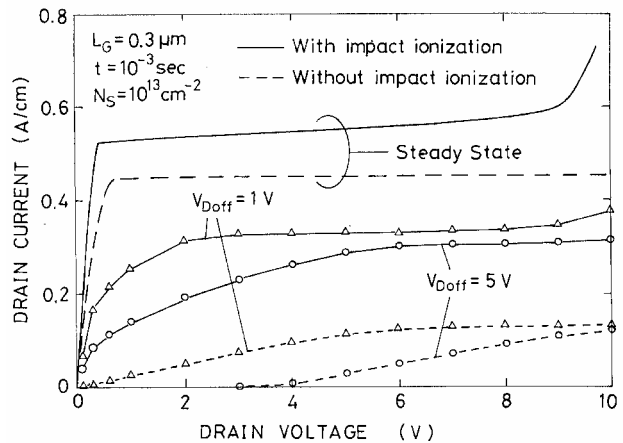

Fig.6. Steady-state I-V curves and quasi-pulsed I-V curves for the case with surface-state densities of 10^{13} cm^{-2}. $V_{Goff} = V_{th}$. (○): $V_{Doff} = 5$ V (corresponds to Fig.5), (△): $V_{Doff} = 1$ V.
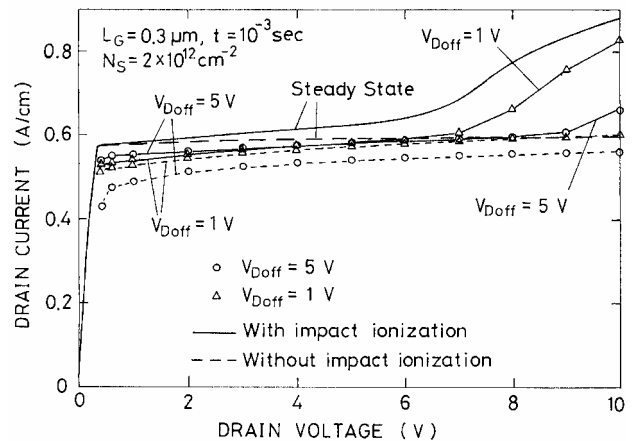

Fig.7. Steady-state I-V curves and quasi-pulsed I-V curves for the case with lower surface-state densities of 2×10^{12} cm^{-2}. $V_{Goff} = V_{th}$. (○): $V_{Doff} = 5$ V, (△): $V_{Doff} = 1$ V.

We have also calculated the case with relatively low surface-state densities. Fig.7 shows the similar pulsed I-V curves for the case with surface-state densities of 2×10^{12} cm^{-2}. In this case, both gate-lag and drain-lag (in the low

voltage region) are small, because the surface-state densities are low. But, the response in the so-called kink region is slow. This indicates that the drain-lag becomes rather large when carries generated by impact ionization themselves become a cause of lag phenomena.

V. CONCLUSION

Effects of substrate traps and surface states (together with impact ionization of carrier) on lag phenomena and pulsed *I-V* curves (or power compression) in GaAs MESFETs have been studied by two-dimensional simulation. It has been shown that the drain-lag occurs mainly due to substrate traps, and gate-lag mainly by surface states. Obtained quasi-pulsed *I-V* curves clearly indicate that the power compression can occur both due to substrate traps and due to surface states, although it may be weaker when impact ionization of carriers becomes important.

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