A Scalable PHEMT Model Taking Into Account Electromagnetic and Electro-Thermal Effects

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***Abstract* — The paper proposes an approach to model a P-HEMT taking into account for the electrical-thermal-electromagnetic behavior in an effective way. The model is based on the integration of a distributed approach, which considers an intrinsic device for gate finger, each of them equipped with a thermal equivalent circuit. The latter considers also the mutual interacting between the adjacent intrinsic devices by means a voltage-controlled voltage-source that allows considering the thermal coupling by a series of coefficients determined in an analytical way. The electrical model has been extracted from a 2x150um PHEMT and then applied to predict the DC and RF characteristic of a 8x150um proving the model scalability capability.**

I. INTRODUCTION

In GaAs PHEMTs used in microwave power amplification, self-heating and electromagnetic intra-coupling effects play a key role; modeling those phenomena becomes necessary to improve the model accuracy and to allow a more accurate design procedure for power devices and MMICs [1]. One of the most important features a model should have is the scalability of the DC and RF parameters with the number of gate fingers and device periphery; on the other hand it is well-know that the scaling rules can be dramatically affected by thermal effects within the device, [1]-[4], that in turn introduces a nonlinear relation between the device geometry and the DC characteristic. In [5] a distributed model was presented to improve the electron device models scalability up to millimeter wave. In particular, the proposed approach has been based on the identification of a convenient number of intrinsic devices connected to a distributed network. Such a network describes the parasitic access network and how the intrinsic devices, which can be described by means of conventional equivalent circuits or other empirical models, interact each other. In this paper, a thermal model is added to the approach proposed in [5]. It considers the mutual thermal interaction between the intrinsic devices through a network composed of thermal resistances connected to equivalent voltage-controlled voltage sources (VCVS) generators, which simulate the thermal exchange between all intrinsic devices and current sources that simulate power dissipation of intrinsic devices. The complete model is capable of taking into account both electro-thermal and electromagnetic effects so that great accuracy in scaling properties is obtained also for those large electron devices used in high power applications where self-heating effects cannot be neglected. The demonstration of this capability is verified in the paper through the prediction of DC characteristic and S-parameter for 8x150um PHEMT manufactured by the OMMIC foundry.

II. THE ELECTRO-THERMAL/ELECTROMAGNETIC MODEL

In order to model thermal effects in an electron device structure, the formal analogy between the thermal diffusion and electromagnetic propagation equations is adopted. This equivalence is effective after a translation in a transformed domain and allows the 3D calculation of the heat diffusion in an analytical way by using a transmission line modeling approach; the description of the method is beyond the scope of this paper and will be published elsewhere [6]. In order to illustrate the idea, a PHEMT having eight 150um-width gate fingers is considered. The result of the thermal analysis for that device is reported in Fig. 1, where the dashed line represents the total temperature distribution as calculated by the method [6], for a median longitudinal section and for a DC power dissipation of 1.2W. The continue curves, in the same figure, refer to the temperature distribution due to the individual intrinsic devices supposed to be isolated by the others. Such a distribution was calculated by the same method but considering a DC power consumption of 150mW (1.2W/8). Finally the thermal resistance R_{TH} is calculated as:

$$R_{TH} = \frac{\hat{T}}{P_d} \tag{1}$$

where $\hat{T}$ is the maximum temperature value, defined with respect to the bulk temperature which is assumed to be constant, "measured" at the finger central point and P_d represented the dissipated power. For the case under investigation the resulting thermal resistance was R_{TH} =120°C/W. From Fig. 1 it is possible to observe that the total thermal distribution is found out by overimposing the individual contributions taking also into account the spacing between elementary thermal sources. It is possible to compute the actual finger temperature weighting the temperatures of all others ones.

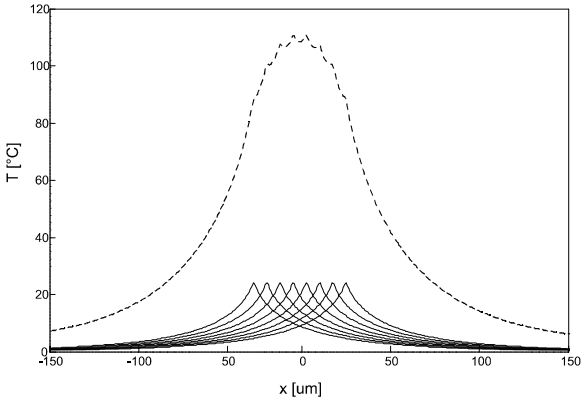

Fig. 1. Thermal distribution calculated in the central section of each finger for the 8x150um PHEMT for a DC power dissipation of 1.3W. Dashed line: resultant thermal distribution; continues lines: singular contribution due to each intrinsic device.

More precisely, once the device structure is completely defined, the contribution of i-th intrinsic device to the j-th is proportional to the temperature of the first and inversely to the mutual distance; this leads to the definition of coupling terms that simply relate the mutual thermal exchange on the basis of their actual temperature and distance. The thermal coupling coefficient matrix is defined by (4). The thermal coupling coefficients have been calculated as:

$$C_{ij} = \frac{T_{FINGERi}}{T_j} \tag{2}$$

where $T_{FINGERi}$ is the temperature of the i-th finger taking into account of the thermal coupling effects, while T_j is the temperature of j-th one in condition of thermal isolation. Using the symmetry of the structure it's possible to write:

$$\begin{aligned} C_{ij} &= C_{ji} \\ C_{i+1,j+1} &= C_{ij} \end{aligned} \tag{3}$$

in table I the values of the coupling coefficient have been reported, for the 8x150um PHEMT considered.

TABLE I
THERMAL COUPLING COEFFICIENTS FOR THE 8X150UM PHEMT

C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}	C_{18}
0.59	0.46	0.37	0.32	0.29	0.25	0.23

$$\begin{bmatrix} T_{FINGER,1} \\ T_{FINGER,2} \\ T_{FINGER,3} \\ \vdots \\ T_{FINGER,8} \end{bmatrix} = \begin{bmatrix} 1 & C_{12} & C_{13} & \cdots & C_{18} \\ C_{21} & 1 & \ddots & \ddots & C_{28} \\ C_{31} & C_{32} & 1 & \ddots & C_{38} \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ C_{81} & C_{82} & C_{83} & \cdots & 1 \end{bmatrix} \cdot \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ \vdots \\ T_8 \end{bmatrix} \tag{4}$$

As reasonably expected the coupling coefficients are decreasing as function of the finger distance. To take into account the self-heating in the PHEMT model, the thermal circuit associated to the intrinsic devices, is composed of the following components. A current-controlled current generator is adopted to transform the DC dissipated power in the equivalent current that flows through the thermal resistance, $R_{TH,i}$. The voltage drop across the resistor in hence added to the potential determined by the VCVSs, which multiples the actual temperature probed from the adjacent intrinsic models, each one including its thermal coupling coefficients. Finally a constant DC sources provides the potential associated the bulk temperature. In this way the multi-finger transistor can be seen as a number of elementary intrinsic models, each one including its thermal circuit and whose interaction with the other devices is described by the VCVSs. The intrinsic models are then connected by the multi-port S-matrix simulating the passive part of the device and computed through electromagnetic simulations. A simplified picture of the circuit is reported in Fig. 2 where is possible to distinguish the arrangement of the thermal model. The thermal profile is performed through a DC analysis.

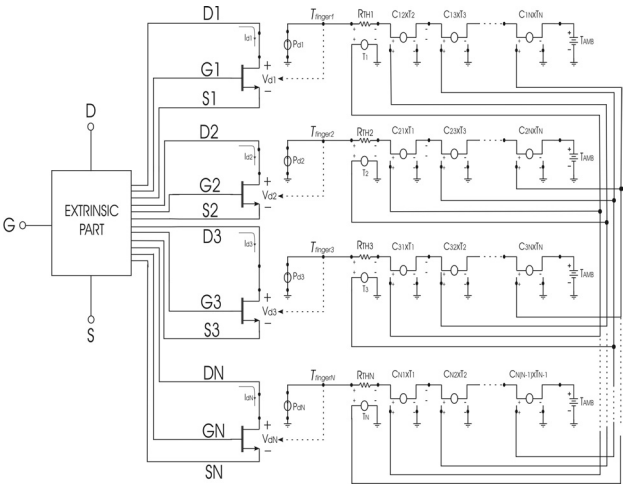

Fig. 2. Simplified schematic of the model for a 2 gate fingers device, showing the extrinsic part, the electrical model and the thermal model

III. DC AND RF SIMULATION AND MEASUREMENT

In order to show the scaling properties of the model, the DC and the RF parameters have been identified for a 2x150um PHEMT, manufactured in the same die of the 8x150um device. The dependence of the model parameter was also characterized. To this end, an external heater was used to heat the device and DC and RF measurement were collected at different temperature. The data have been then used to fit the variation of the Idss, and Vt with the temperature, while for Rs,Rd,Cgs and Cds a meaningful temperature dependence was not observed.

Fig. 3 show the comparison between simulations, with and without thermal effect, and measurement for the 2x150um PHEMT device used to identify the intrinsic device model, while Fig. 4 shows the prediction of the DC characteristics for the 8x150um PHEMT in the same condition, compared with measurement. It must be outlined that the model for the 8x150um device was obtained by using the intrinsic device model determined

by fitting procedure recalled above, in conjunction with proper e.m. characterization of the 8x150um extrinsic part [5]. The quite important self-heating effects on the DC curves is evident for high values of the current, in particular for the larger device; the accuracy of the model and scalability is allowed only by thermal model described above. If the thermal model was disabled the curves would appear with a marked positive slope diverging considerably from the measurement (not shown).

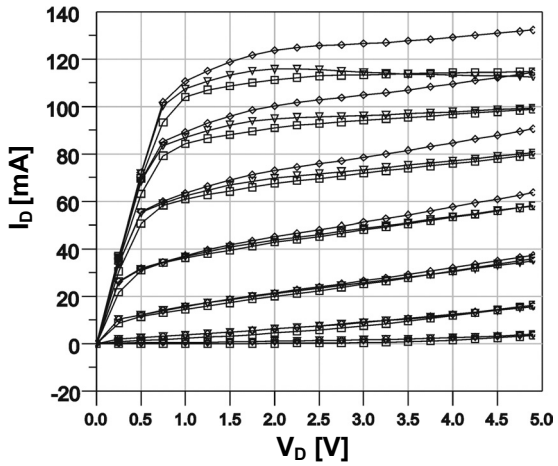

Fig. 3. DC Comparison between simulation (triangle) with thermal effect, simulation without thermal effect (diamond) and measurement (square), for the 2x150um PHEMT

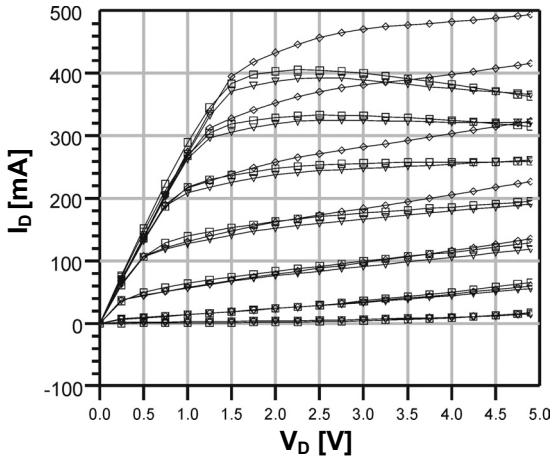

Fig. 4. DC Comparison between simulation (triangle) with thermal effect, simulation without thermal effect (diamond) and measurement (square), for the 8x150um PHEMT

The model's dynamic parameters have been extracted by small-signal measurement for the 2x150um device and the used to predict the small-signal performance of the 8x150um device. Also in this case there is a good agreement between measurement and simulation for both the devices (bias point Vd=3V and Vg=-0.45V) Fig. 6 and Fig. 7. Similar result have been obtained for various bias points.

VI. Conclusion

In this paper an approach has been proposed to model PHEMTs with large gate periphery taking into account the electro-thermal/electromagnetic behavior in an effective way. The model is based on a distribuited approach allowing scalability properties. The feature has been proved by extracting the intrinsic device model from a 2x150um PHEMT. The same intrinsic device model was the used to predict the DC and RF characteristic of a 8x150um device. DC and S-parameter measurement were provided to validate the model. The approach is suitable for MMIC design, optimization of PHEMT extrinsic structures and is a starting point for the model extension to large signal operations.

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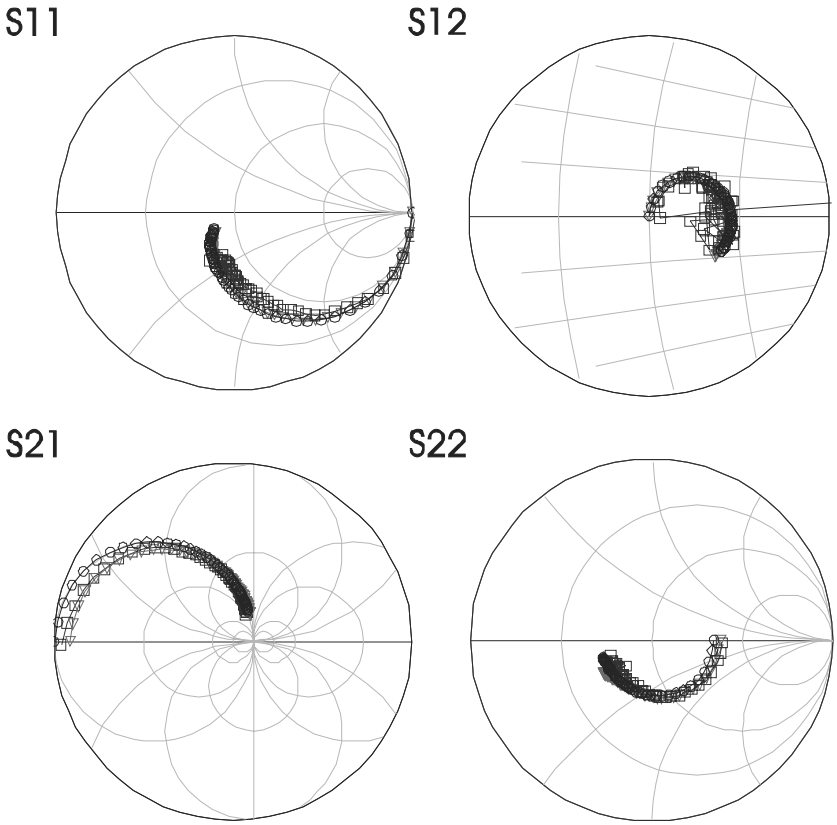

Fig. 6. S parameter Comparison between simulation (triangle) with thermal effect, simulation without thermal effect (diamond) and measurement (square), 2x150 pHEMT from 100MHz to 20GHz

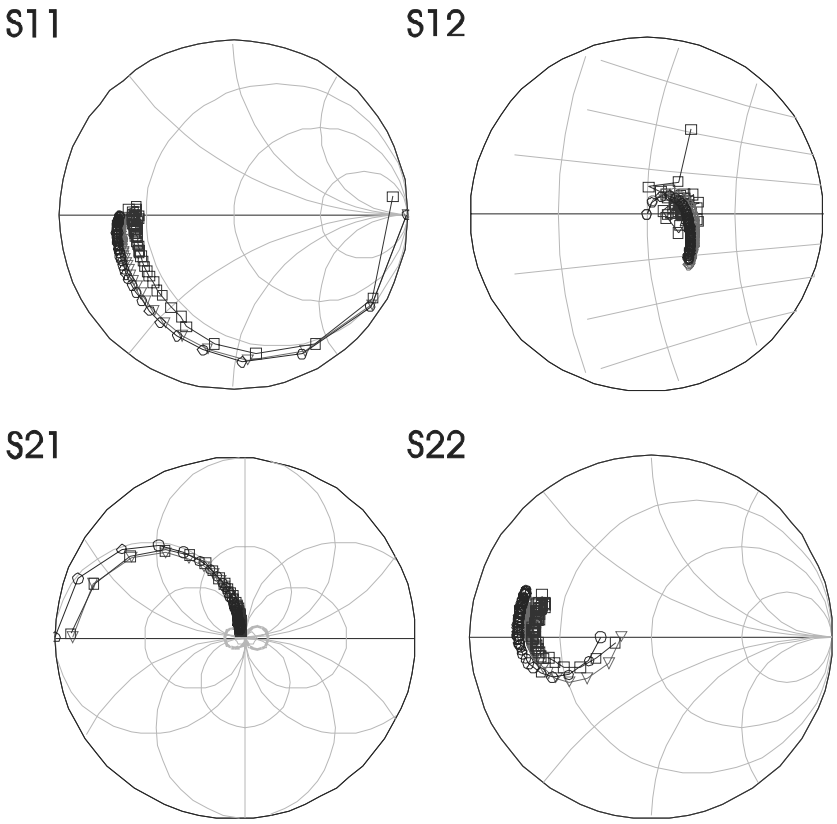

Fig. 7. S parameter Comparison between simulation (triangle) with thermal effect, simulation without thermal effect (diamond) and measurement (square), 8x150 pHEMT from 100MHz to 20GHz.