Low Loss On-chip Passive Components for Si-MMIC by Using CPW Structure

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ABSTRACT

Si-MMIC's become the key components to realize low cost single chip RF sections for mobile communication terminals. To realize on-chip matching Si-MMIC's, there is a problem of high-loss on-chip passive components due to the dielectric loss of Si substrates. In the conventional Si-IC process used for analog/digital IC production, low resisivity Si substrates have been used, and it is difficult to change to high resistivity Si substrates. Based on electro-magnetic simulation, the loss reduction effect by using coplanar waveguide (CPW) structure is analyzed for low resistivity Si substrates. The measured results of transmission lines and on-chip spiral inductors show the superiority of CPW over microstrip line (MS).

INTRODUCTION

Due to the recent and rapid expansion of wireless communication markets such as cellular phones, Si based RF-IC's have been focused as strategic devices for handset industries to realize low production cost and small size terminals [1]-[3]. The main features of Si-MMIC for wireless terminals are follows; (1) low production cost comparing with GaAs-IC's especially for very large number mass production, (2) feasibility of system on a chip or single transceiver chip which enable to realize ultra-small size terminals.

In terms of (1) low production cost, the chip cost is several times lower than GaAs-IC's, but the conventional Si process must be used. And also, in terms of (2) feasibility of system on a chip, the process of Si-MMIC must have compatibility with the conventional Si analog/digital IC's. To realize single transceiver chip, almost all RF sections must be integrated, therefore low loss inter-stage matching circuits or bias circuits must be fabricated on Si chip. Since the conventional Si processes need to use low resistivity Si substrates, on-chip RF passive circuits for matching / bais circuits are lossy due to dielectric loss of low resistivity Si substrates [1].

In the case of low resistivity Si substrate, CPW structure shows dielectric loss reduction effect [1], [4], [5]. In this paper, the loss reduction effect is analyzed by using electro-magnetic simulation. Electric filed distribution inside of Si substrate is also discussed. The simulated results for transmission lines are evaluated by the measurements. The measured results of on-chip spiral inductors shows that the use of CPW structure is one of the solutions to realize low loss on-chip RF passive circuits on low resistivity Si substrate.

ANALYSIS OF TRANSMISSION LINE BY USING ELECTRO-MAGNETIC SIMULATION

In this section, two loss reduction ways are described with referring simulated results of electro-magnetic analysis. One is the use of coplanar wave guide (CPW) structure [1]. In comparison with microstrip line (MS) structure, both simulated and measured CPW type transmission line has lower loss than MS type. Another is the use of other type Si substrate, such as high resistivity Si substrate [6] or SOI substrate [7]. By using these substrates, effect of dielectric loss of the substrate can be reduced.

In order to discuss the loss of transmission lines on various Si substrates, characteristics comparison between six transmission line configurations has been carried out by using electro-magnetic simulation:

(i) MS structure on semi-insulated (ρ =1M Ω : this is an ideal model and is almost same as GaAs-MMIC) substrate.

(ii) MS structure on low resistivity (ρ=50Ω*) substrate. (* is an extracted value at 2GHz. At d.c., ρ =10-20 Ω.)

(iii) MS structure on SOI substrate. (Bulk: ρ=50Ω*)

(iv) MS structure on high resistivity (ρ =1k Ω) substrate.

(v) CPW structure on low resistivity substrate.

(vi) CPW structure on high resistivity substrate.

Cross sectional views of the transmission lines are shown in Fig.1. To make comparison simple, substrate thickness was 400μm and strip line width (W) was 30μm. For CPW transmission line, gap between strip line and grounded metals (S) was designed as 20 μm to obtain 50 Ω characteristic impedance. Table 1 shows the conditions of each transmission lines, and Table 2 shows electro-agnetic simulation results of transmission lines (i)-(vi). Cross sectional views of calculated electrical field distributions are shown in Fig.2.

Case (i) is an ideal case, and the electric field distribution shown in Fig.2(a) is normal. In the case of (ii), since the substrate resistivity is low, the electric field does not come into the substrate sufficiently as shown in Fig.2 (b), and equivalent ground plane of MS can not be the backside of substrate but inside of substrate.

Therefore, the loss is relatively higher and the characteristic impedance is relatively lower than that of MS line (i) or (iv). In the case of SOI (iii), calculated results are almost same as the case (ii) as shown in Fig.2(c).

Difference of transmission characteristics between (i) and (iv) is fairly small, and high resistivity Si substrate can be used instead of GaAs like semi-insulated substrate as shown in Fig.2(d). As the results, the use of high resistivity substrate is quite effective way to reduce the loss of transmission line on Si substrate.

In the case of CPW (v), since the electrical field is concentrated at the gap between strip line and grounded metals as shown in Fig.2(e), it does not go into the lossy substrate deeply and the CPW (v) has 50% lower loss than that of MS (ii). The use of CPW structure instead of MS is effective for the loss reduction of passive circuits on low resistivity Si substrate. Even in the case of CPW on high resistivity Si substrate (vi), its loss is not exceeded that of MS (iv) on the same resistivity substrate. In both cases, (v) and (vi), there are grounded plane existed on the backside of the substrate, but they don't affect the transmission line characteristics. Therefore, transmission lines (v) and (vi) can be considered as CPW.

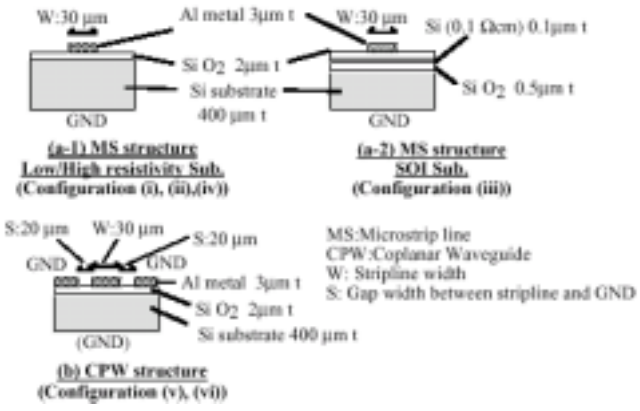
Table 1 Conditions of various transmission lines.

Substrate		MS structure	CPW structure
Semi-insulated substrate	(ρ=1MΩcm*)	(i)	
Low resistivity substrate	(ρ=50Ωcm**)	(iii)	(v)
SOI substrate (low resistivity Si)	(ρ=50Ωcm**)	(iii)	
High resistivity substrate	(ρ=1kΩcm)	(iv)	(vi)

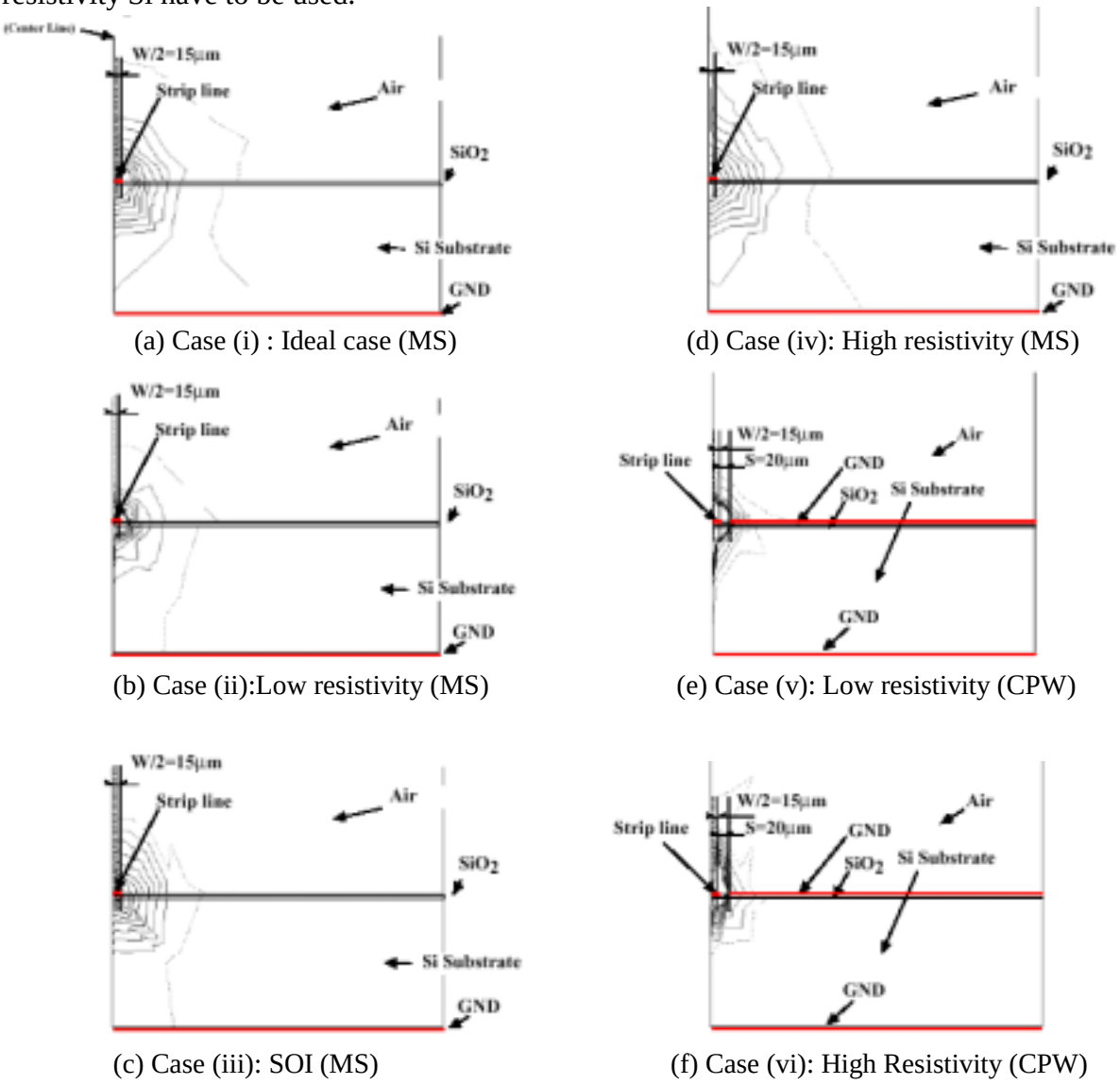
* : ideal model, almost same as GaAs-MMIC.

** : extracted value at 2GHz. At d.c., ρ=10-20Ωcm.

Fig.1 Cross sectional views of various transmission lines for electro-magnetic simulation.



As the results, the use of CPW structure is one of the effective ways to reduce the loss of passive circuits on low resistivity Si substrate. But, to reduce the loss to the GaAs-MMICs level, high resistivity Si have to be used.



(a) Case (i) : Ideal case (MS)

(d) Case (iv): High resistivity (MS)

(b) Case (ii):Low resistivity (MS)

(e) Case (v): Low resistivity (CPW)

(c) Case (iii): SOI (MS)

(f) Case (vi): High Resistivity (CPW)

Fig.2 Cross sectional views of calculated electrical field distributions of various transmission lines.

Table 2 Electro-magnetic simulation results of transmission lines (i)-(vi).

Type	Transmission line structure	Si substrate	Resistivity ρ (Ωcm)	Loss (dB/mm)	Z0 (Ω)	λo/λg
(i)	Microstrip line	Semi-insulated (GaAs compatible)	10^6	0.03	112	2.7
(ii)		Low resistivity	50	0.54	78	3.2
(iii)		SOI	50	0.55	80	3.2
(iv)		High resistivity	10^3	0.05	112	2.7
(v)	Coplanar waveguide	Low resistivity	50	0.33	43	2.9
(vi)		High resistivity	10^3	0.05	55	2.3

(CPW is very easy to realize characteristic impedance of 50Ω.)

MEASURED RESULTS

In order to evaluate the analytical results, three types of transmission lines are fabricated. Table 3 shows the comparison between calculated and measured results for these transmission lines. Good agreement between these data shows the reliability of electro-magnetic simuation results and the discussion.

Fig.3 shows the insertion loss of fabricated MS and CPW type on-chip spiral inductors on low resistivity Si substrate. The measured results show that loss reduction effect can be obtained in the case of on-chip passive components.

Table 3 Comparison between calculated and measured results of transmission lines

[ ]: Calculated results by EM simulation

Type	Transmission line structure	Si substrate	Loss (dB/mm)	λo/λg
(iii)	Microstrip line	Low resistivity	0.59 [0.54]	3.5 [3.2]
(iv)		High resistivity	0.08 [0.05]	2.7 [2.7]
(v)	Coplanar waveguide	Low resistivity	0.20 [0.33]	3.5 [2.9]

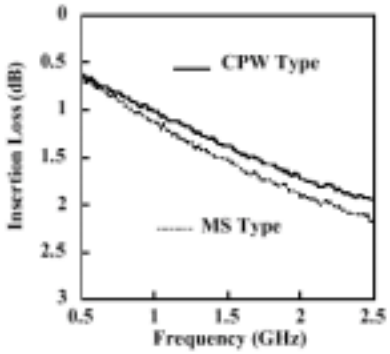


Fig.3 Insertion loss of fabricated MS and CPW type on-chip spiral inductors on low resistivity Si substrate.

CONCLUSION

The latest Si process has led Si MMIC's to the practical use for mobile communication terminals. To make full use of Si-MMICs merits, the integration of RF / IF / Base Band circuits is the key issue. For the integration of RF sections, achievement of low-loss on-chip passive circuits is quite important.

In this paper, low-loss on-chip passive circuit techniques are described. One is the use of CPW structure and another is the use of high resistivity Si substrate. Based on the electro-magnetic simulation results, it is shown that the use of CPW is effective when low resistivity Si substrate has to be used. This discussion is evaluated by the measurements of fabricated transmission lines and on-chip spiral inductors.

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