Harmonic Distortion Characterization of SOI MOSFETs

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***Abstract*— Harmonic Distortion (HD) of Partially and Fully Depleted Silicon-on-Insulator nMOSFETs is investigated through DC and Radio-Frequency (RF) characterization methods. Those techniques are compared and it demonstrates that in saturation, HD is dominated by the DC current-voltage characteristics and that the output conductance has to be taken into account. Accurate evaluation of HD at RF requires further measurements.**

I. Introduction

The performances of microwave transceivers depend on the knowledge of their non-linear behavior. As Silicon-on-Insulator (SOI) is one of the most promising low cost technology for integrated low-voltage, low-power circuits operating at microwaves [1], we focus on the distortion characterization of SOI nMOSFETs.

Several techniques to measure and characterize the distortion of a MOSFET are already available. Some are based on the measured output DC curves, by applying Fourier series analysis via the calculation of high-order derivatives of the $I_D(V_D)$ and $I_D(V_G)$ characteristics [2]. More recently, an integral function method (IFM) [3], [4] was proposed with the advantage to be less sensitive to the measurement noise than Fourier series analysis. While those are cheap and rapid techniques, they neglect the non-linearities associated with memory and high-frequency effects. Other techniques based on RF measurements require more specific equipment as a sampling oscilloscope or a Large-Signal Network Analyser (LSNA) [5]. This last technique offers full characterization as we get both phase and amplitude of the signal, at the price of an expensive and non-widespread experimental set-up.

The origin of nonlinearities are explained by the semiconductor physics. The DC drain current exhibits a highly nonlinear characteristic as a function of the applied voltages [6]. At high frequency operation, the effect of capacitances is no more negligible and also introduces nonlinearities. Furthermore in new technologies dedicated to high-frequency, the dimensions are shrunk and other linearity degradations linked to short channel effects and parasitics appear. So carrier velocity saturation, channel length modulation, series resistances and mobility degradation have to be taken into account for an accurate large signal RF modeling of the MOSFET [7].

We compared the harmonic distortion (HD) behavior of SOI nMOSFETs using both IFM and LSNA measurement techniques. The used de-embedding procedure for high frequency measurements is described in [8]. We checked that it gives good agreement with classical Through-Line-Reflect method and that the level of applied power has no influence on the passive devices on silicon substrate. A set of scattering parameters of the calibration kit elements may so be used for the de-embedding purpose.

The devices under test (DuT) that are considered through the present analysis, are Partially-Depleted (PD) and Fully-Depleted (FD) SOI nMOS composed of 12 fingers connected in parallel, 6.6 μm width and 0.25 μm length each, built at CEA-LETI, France, following a 0.25 μm process. The extracted threshold voltage V_{th} are 0.56 V and 0.41 V, for PD and FD devices, respectively. All measurements were performed on-wafer with the source of the MOSFET grounded. Even if we are aware that intermodulation distortion (IMD) is also an important parameter for most microwave applications, only one-tone analysis will be considered in this work. However, IMD is directly related to HD by simple relations in the case of weak nonlinearities of memoryless circuits [2].

II. Nonlinear analysis

In this section, we provide the extraction of the non-linear characteristics of PD and FD SOI MOSFETs in saturation mode from weak to strong inversion.
Consider a 900 MHz (f_o) signal of magnitude $V_o = 0.2$ V applied to the gate of the transistor:

$$V_g(t) = V_G + V_o \sin(2\pi f_o t) \tag{1}$$

Total Harmonic Distortion (THD) of our FD device extracted with both LSNA and IFM methods is shown in Fig. 1. Note that RF measurements were performed on a 50 Ω system while the load impedance of the transistor is considered to be infinite for the DC measurements used by IFM. The THD extracted from the IFM is directly related to the output current while at RF, we used the following definition of THD:

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} \Re(V_{out,n} \cdot I_{out,n}^*)}{\Re(V_{out,1} \cdot I_{out,1}^*)}} \tag{2}$$

where $V_{out,n}$ and $I_{out,n}$ are the voltage and current of the n^{th} harmonic, respectively.

From 0.2 V up to 0.8 V both methods give THD results in agreement. LSNA and IFM methods present a THD minima which depends on the drain bias condition, however IFM shows minima at higher V_G corresponding actually to the inflection point of the $I_D(V_G)$ curve, i.e. the maximum of the gate transconductance, whereas at RF the minimum of THD is no more only linked to the DC characteristic, as capacitances

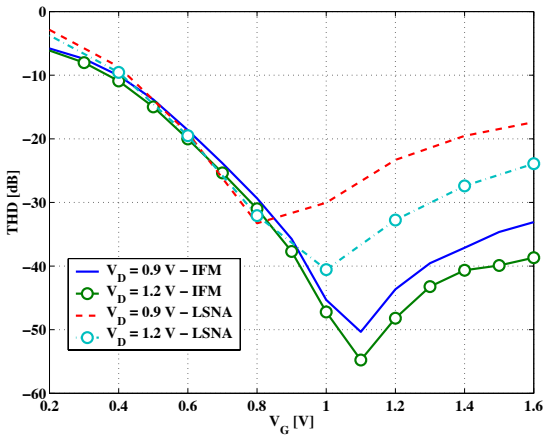

Fig. 1. THD of the FD device measured with LSNA and calculated by IFM for various drain voltage; the AC input signal V_o is 0.2 V.

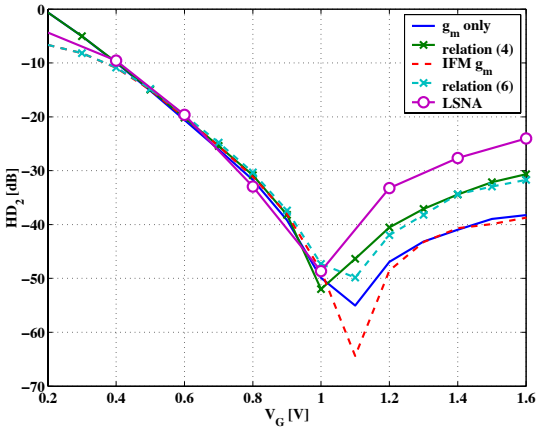

Fig. 2. HD_2 of the FD device measured with LSNA and calculated with the help of relations (4) and (6); the AC input signal V_o is 0.2 V and the drain bias is 1.2 V.

get importance. Therefore, the gate voltage at which the THD reaches its minimum extracted from RF measurements corresponds to the maximum gain G_P of the transistor, defined as $G_P = \left|\frac{(V \cdot I^*)_{output}}{(V \cdot I^*)_{input}}\right|_{f=f_o}$.

With the IFM the distortion extracted from the $I_D(V_G)$ curve is only related to the THD of the transconductance g_m (Fig. 1). However, the LSNA analysis takes all the elements of an equivalent circuit into account (transconductance, output conductance and capacitances). So, to characterize the HD with better accuracy, we need to take the distortion of the output conductance g_d into account [9]. In order to get a analytic formulation of HD at low frequencies, it is assumed that the drain current of the MOSFET is expressed:

$$\begin{aligned} I_D(t) &= I_{D0} + g_{m1}V_g(t) + g_{m2}V_g^2(t) + g_{m3}V_g^3(t) \\ &\quad + g_{d1}V_d(t) + g_{d2}V_d^2(t) + g_{d3}V_d^3(t) \end{aligned} \quad (3)$$

This assumption holds when the device is saturated, however in the triode mode, cross-derivative terms should be added [9]. In the case of weak nonlinearities, considering that $V_d(t) = (g_{m1}/Y_L^{'})V_g(t)$, the harmonic distortion of order two HD_2 and three HD_3 may then be approximated by:

$$HD_2 = \frac{V_o}{2}\left|\frac{g_{m2}}{g_{m1}} + A_{vDC}\frac{g_{d2}}{Y_L^{'}}\right| \quad (4)$$

$$HD_3 = \frac{V_o^2}{4}\left|\frac{g_{m3}}{g_{m1}} \quad A_{vDC}^2\frac{g_{d3}}{Y_L^{'}}\right| \quad (5)$$

where $A_{vDC} = g_{m1}/Y_L^{'}$ and $Y_L^{'} = Y_L + g_{d1}$, Y_L being the load admittance of the MOSFET. The parameters g_{mi} and g_{di} can be obtained by differentiation of the $I_D(V_G)$ and $I_D(V_D)$ curves. Equations (4) and (5) allow us to analyze the influence of the load on HD. For a low load impedance, distortion of the transconductance dominates while for higher level of impedance, the output conductance also affects the HD. On the other hand, as we may extract HD_2 of g_m and g_d separately by IFM, it follows from (4) that:

$$HD_2 \leq HD_{2,g_m}^{IFM} + \left(\frac{1}{1+\alpha}\right)|A_{vDC}| \cdot HD_{2,g_d}^{IFM}. \quad (6)$$

where $\alpha = Y_L/g_{d1}$ and $HD_{2,g}^{IFM}$ is assumed to be equal to $\frac{V_o}{2}\left|\frac{g_2}{g_1}\right|$ as suggested in [3]. This last expression present the advantage compared to (4) that only the first derivatives of the I V characteristics have to be calculated. Fig. 2 compares HD_2 evaluated with the help of relations (4) and (6) with the sole contribution of g_m to HD_2 and LSNA. In the calculations, the load impedance is set to 50 Ω and the considered signal amplitude V_o is 0.2 V in order to assure the validity of expressions (4) and (5). As the two terms in the norm of equation (4) are both positive, we get equality in (6). Furthermore, if the output conductance is taken into account, the gate bias at which the minimum occurs is evaluated with better accuracy.

In Fig. 3 and Fig. 4, we plotted the contribution to THD of the transconductance and the output conductance extracted from IFM for FD and PD devices, respectively. Taking both contributions into account, the obtained curve is closer to the LSNA measurements. It indicates again that the effect of output conductance is not negligible, specially at high V_G, i.e. close to the triode mode.

If the transistor is excited at still higher frequencies, the LSNA measurements show that the distortion does not vary much (Fig. 5). Due to the low pass characteristic of MOSFET, harmonics at high frequencies are filtered, leading to a global lower level of distortion. Indeed, the capacitances seen at high frequencies do not generate any significant nonlinearities [9], but they affect the output impedance and swing. Note that self biasing was not considered through this analysis.

Both LSNA and IFM allow to extract the harmonic voltage intercept points of order three (VIP_3). The extraction with IFM is based on the assumption that the signal amplitude A is very low so that the relation (7) holds.

$$VIP_3 = 2\sqrt{\left|\frac{g_{m1}}{g_{m3}}\right|} \quad (7)$$

If measurement data are used, IFM is far more robust that the direct evaluation of (7) as no derivatives are needed. On the other hand, the evaluation of the VIP from the plot of output power *vs* input power measured at RF is very sensitive to the interpolation of the linear part of the curves. As shown in

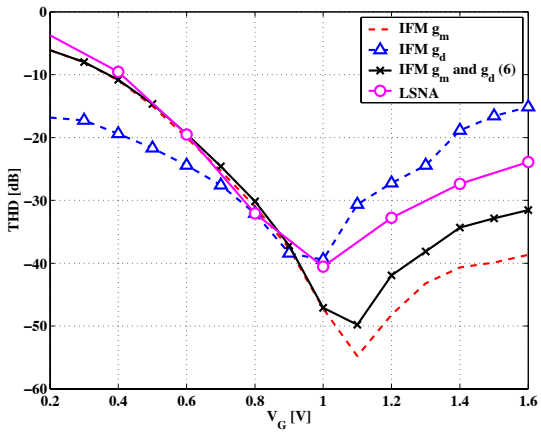

Fig. 3. THD from IFM applied on $I_D(V_G)$ ($\triangle$), $I_D(V_D)$ (o) and the sum of those contributions (-) compared to LSNA measurements (x), $V_D = 1.2$ V, $V_o = 0.2$ V, FD SOI MOSFET.

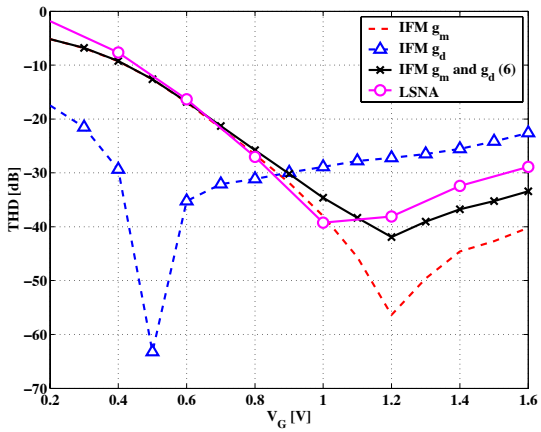

Fig. 4. THD from IFM applied on $I_D(V_G)$ ($\triangle$), $I_D(V_D)$ (o) and the sum of those contributions (-) compared to LSNA measurements (x), $V_D = 1.2$ V, $V_o = 0.2$ V, PD SOI MOSFET.

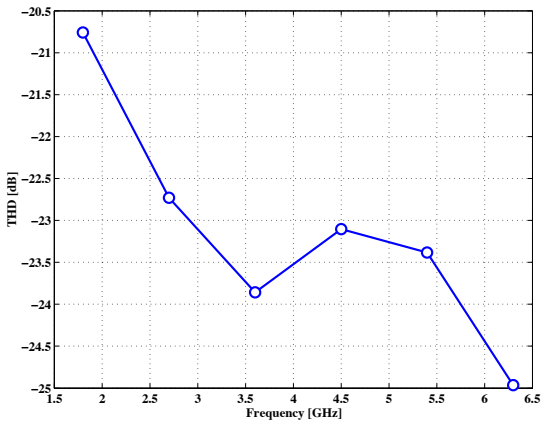

Fig. 5. Influence of frequency on the distortion, $V_D = 1.2$ V, $V_G = 1.2$ V, $V_o = 0.2$ V, PD device.

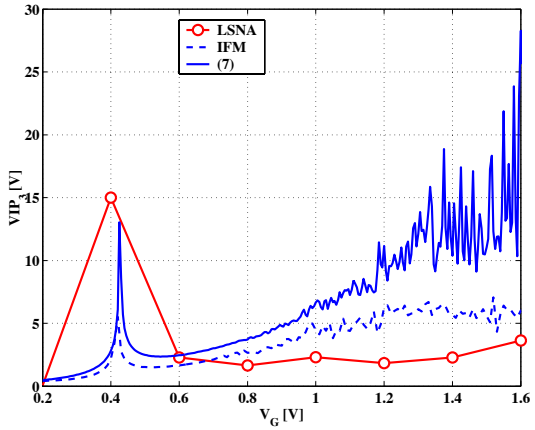

Fig. 6. VIP_3 of the FD device as extracted from IFM, LSNA and equation (7); the drain bias is set to 1.2 V.

Fig. 6, there is a good agreement between the methods for bias voltages where the effect of g_D is negligible. So IFM provides a quick, simple and valuable evaluation of the intercept points. Furthermore, the peak around the threshold voltage is still present at RF. As in practical cases, balanced circuits are use to cancel even order distortions, this means that biasing the transistors in the moderate inversion improves the linearity of the devices.

III. Comparison between FD and PD SOI nMOS

The large signal analysis was performed on both PD and FD devices. In Fig. 8, a comparable level of HD_3 is again observed for both DuT. As the gate bias exceeds 0.8 V, the effect of the output conductance has to be taken into account for better description of the HD from the DC measurements. The minimum peak occurs at the threshold voltage of each device, as it is the inflection point of the transconductance plot.

In order to get the same degree of inversion in the channel, we plotted in Fig. 7 the THD of the devices in function of the transconductance over drain current ratio. No major differences are noted except close to the minimum in Fig. 1. A lower level of THD is then expected from the DC characteristic for both PD and FD devices, as explained before.

It is worth noting that the output conductance of PD SOI MOSFET depends on both bias and frequency. As the kink effect vanishes at high frequencies, same level of nonlinear performances are expected at RF for both kind of devices. The impact of the frequency dependence on the IMD of the transistor had been discussed in [10].

IV. Conclusion

The characterization of the harmonic distortion of SOI nMOSFETs was performed using the DC characteristic by the integral function method (IFM), and RF large signal measurement technique. We showed that at 900 MHz, when the gate bias is varied, HD is dominated by the DC I_D V_G characteristic up to 0.8 V for our sample. The observed THD minimum is shifted to lower gate bias voltages as the frequency is increased. At low frequencies, the minimum of THD-VG is determined by the maximum of the appropriated transfer function, which is the power gain at RF. Furthermore,

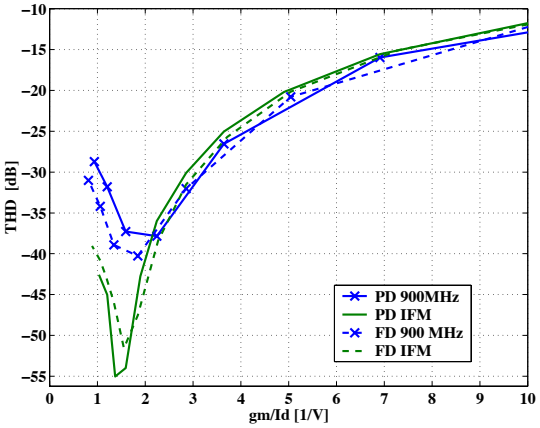

Fig. 7. Comparison of the THD of PD and FD SOI MOSFETs, the IFM case does not take the effect of output conductance; $V_D = 1.2$ V, $V_o = 0.2$ V.

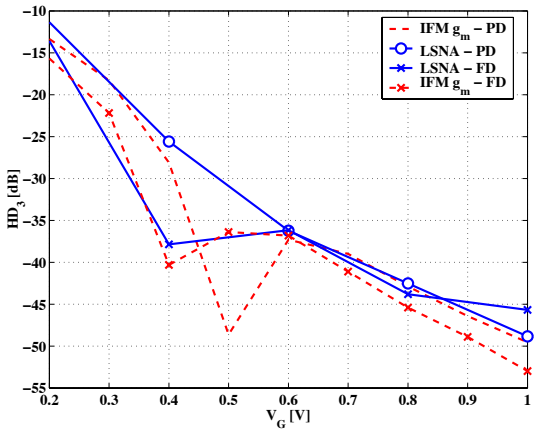

Fig. 8. FD and PD devices exhibit same level of HD_3 for $V_G < 0.8$ V. $V_D = 1.2$ V, $V_o = 0.2$ V.

better accuracy is obtained if the distortion of the output conductance is taken into account.

In saturation, FD and PD SOI MOSFETs exhibit the same level of distortion.

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