Global modeling approach to the design of an MMIC amplifier using Ohmic Electrode-Sharing Technology

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***Abstract* — An innovative technique for high-density, high-frequency integrated circuit design is proposed. The procedure exploits the potentialities of a global modeling approach, previously applied only at device level, enabling the circuit designer to explore flexible layout solutions aimed at important reduction in chip size and cost. The new circuit design technique is presented by means of an example consisting of a wide-band amplifier, implemented with the recently proposed Ohmic Electrode-Sharing Technology (OEST). The good agreement between experimental and simulated results confirms the validity of the proposed MMIC design approach.**

I. Introduction

The development of high-performance, low-cost monolithic micro- and millimeter-wave integrated circuits requires more powerful design techniques being able to take into account the strong and important coupling phenomena usually existing in complex and dense structures. It is a matter of fact that the use of standard approaches based on conventional circuit simulations by means of component libraries supplied by the foundry, allows a limited accuracy in predicting the performance of such a kind of circuits. In order to overcome this constraint a global design procedure is required, where the effects of the passive parts as well as the interactions with active devices have to be consistently taken into account. . This goal can be obtained by an accurate electromagnetic simulation (EM) of the complete passive parts of the circuit, including the FET metallizations, and a proper characterization of the *intrinsic* part of the active device. The EM simulations are based on the effective layout and substrate parameters while the *intrinsic part* is identified by means of the global modeling approach presented in [1,2].

The predictive capabilities of the method lead to the possibility of designing high-density integrated circuits, which may consist of unconventional configurations where active and passive devices are closely spaced in order to get compact size and low production costs. In particular, the adopted design approach allows the performance prediction of MMIC structures designed on the basis of the ohmic electrode-sharing technology (OEST) [3].As well known, this kind of circuits cannot be simulated by simply using conventional CAD tools and standard libraries. In the present paper the method is applied to the amplifier configuration shown in Fig.1, but no drawback exists in applying it to all the different families of circuits whose design can take advantage from size-shrinking and the use of a distributed, scalable linear FET model providing accurate bias-dependent S-parameters.

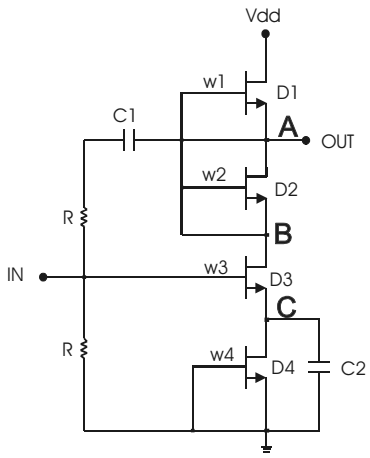

Fig. 1. Schematic of the designed amplifier.

II. Circuit Design and Analysis

By considering the amplifier in Fig.1, a conventional approach requires a layout implementation with four different FETs interconnected through transmission lines. Instead, the alternative and unconventional layout presented here is based on the Ohmic Electrode-Sharing Technology (OEST) [3]. This enables all the interconnecting lines between cascaded FETs to be removed because the ohmic electrodes of two adjacent FETs with the same electric potential are realized with a single electrode, obtaining a drastic reduction of the chip size as well as a decrease of the transmission losses.

With reference to Fig.1, the ohmic electrode labeled ‘A’ and shared by the series FETs D1 and D2 is the drain of D2 and the source of D1. Analogously, the ohmic electrode labeled ‘B’ is the source of the FET D2 and the drain of the FET D3; the electrode ‘C’ acts in the same way for D3 and D4, respectively. The typical OEST implementation of such a topology is shown in Fig.2, where the labels have the same meaning as in Fig.1. The dimensions of each single gate FET have been chosen in order to optimize the circuit performances starting from a basic configuration with four 30 um gate width FETs. The optimization process has involved only D1 and D3 devices (w1, w3 respectively), as shown in Tab.1, while the active loads D2 and D4 have been fixed at 30 um gate width (w2, w4). In order to predict MMIC performance

versus circuit layout and geometry-related FET parameters, the approach proposed in [1] was used. This approach was successfully applied in [1,2] to predict FET performance up to millimeter-waves, as a function of gate width and finger number, leading to the development of a distributed, scalable linear FET model dependent on the bias point. The same technique enables the performance of MMIC's based on unconventional layout structures to be predicted.

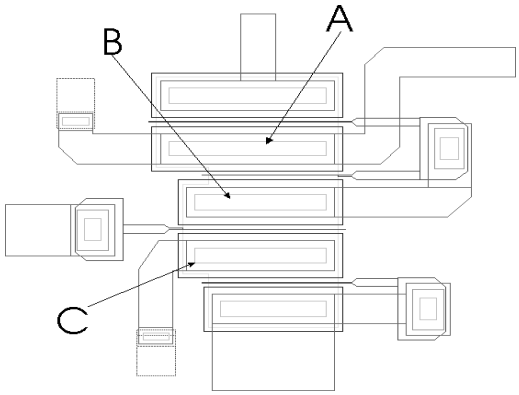

Fig.2. Detail of the OEST structure for the amplifier described in Fig.1.

For each case listed in Tab.1, an electromagnetic (EM) simulation of the complete amplifier layout was performed by means of the Agilent ADS2002 "Momentum" simulator [4]. The aim is the full characterization of the passive part of the circuit by means of a multi-port scattering matrix description (including DC) taking into account the bonding-pad areas and considering the geometries and material stratification as well as losses in the dielectrics and electrode structures.

	W1	W3
Case A	30	30
Case B	30	35
Case C	30	40
Case D	35	30
Case E	35	35
Case F	35	40
Case G	40	30
Case H	40	35
Case I	40	40

Tab1. D1, D3 gate width optimization.

The process parameters were available from the design rules provided by the foundry [5]. The bias points of D1, D2, D3 and D4 for each case listed in Tab.1 were determined by connecting the internal port of the circuit passive part with a simple scalable model fitting the DC characteristic of the active part of the device.

For each of the selected bias point the intrinsic part of the active devices have been characterized in terms of an admittance matrix per gate-width unit. The Y matrix corresponding to a certain gate width has been obtained by properly scaling the unitary gate-with matrix to the actual gate width. [1,2]

The admittance description of the "intrinsic active slices" [1,2] in conjunction with the "extrinsic", distributed S-matrix representation, enables the MMIC performance to be predicted taking into account complex electromagnetic effects and interactions between active devices.

The whole circuit description, combining the active and passive circuit parts in terms of AC (Y- or S-parameter) data-components , was implemented in Agilent-ADS2002 [4] in order to perform the small-signal S-parameter MMIC analysis. To this aim it is important to observe that, in the modeling of electrically distributed systems using a circuit representation, one of the main issues is the assignment of the system reference potential. Usually circuit simulators adopt a nodal approach where voltages are assigned to nodes and each of these voltages is referred to a common reference point, commonly called "ground". In a spatially distributed structure, when the separation between two adjacent nodes is a significative fraction of the wavelength, it is not possible to define a unique voltage and consider it as common reference point. In that sense port voltages of any elementary device are referred to a "local potential" depending on the distributed passive network which could be considered as an additional state variables. In order to overcome this problem the concept of "local reference nodes" [6] was introduced in the model implementation.

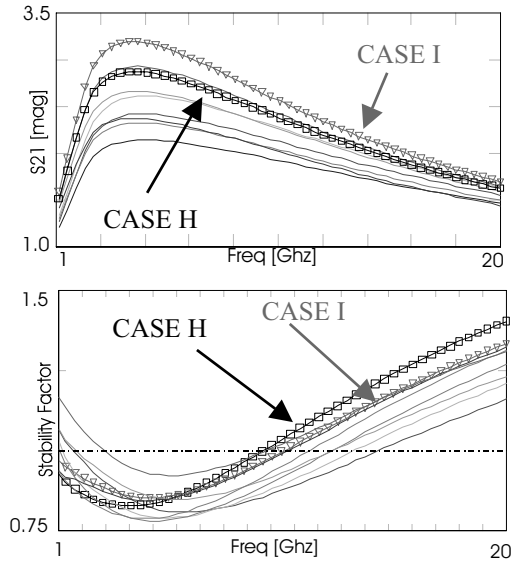

Fig. 3. S21 parameter and Stability Factor of each case in Tab1 (case H: square; case I: triangles; all others cases: lines).

In Fig3, simulation results of the complete amplifier are shown for each of the cases listed in Tab1. By considering a trade off between S21 magnitude and stability factor K, the best performances are provided by

case H, corresponding to gate widths 40um e 35um for D3 and D1 respectively.

The amplifier was designed using the OMMIC ED02AH GaAs 0.2µm P-HEMT process. The layout of the MMIC amplifier, realized with the selected gate widths (w2 = w4 = 30um, w1 = 40um; w3 = 35um) is shown in Fig.4. The total chip area, including contacting GSG pad areas, is 0.38x0.36mm^2, while the four FETs of the OEST configuration are integrated into an area of 0.12x0.10mm^2 having a highly compact structure. The conventional layout of the same amplifier, designed using four "separated" active devices, would occupy an integrated area of 0.3x0.2mm^2, without GSG pads area. Thus, the OEST allows a chip size reduction of about 80% in comparison with the conventional layout design.

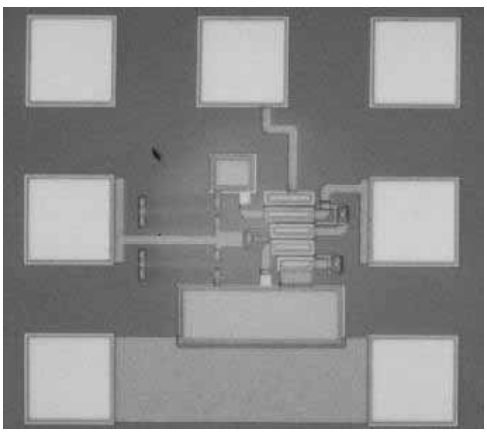

Fig. 4 Amplifier prototype (0.38x0.36mm^2).

III. Experimental results

An on-chip characterization of the proposed amplifier was carried out. The scattering parameters were measured directly on-wafer up to 20GHz using an HP8510C network analyzer. Figs.5a and 5b show the comparison between on-chip S-parameter measurements in the 1-20 GHz range and the corresponding simulations carried out with both the proposed method and the standard libraries. The simulation results obtained with the approach proposed in this paper show a very good agreement with measurements, while library-based results highlight an accuracy degradation at higher frequencies. The most important characteristic is the highly accurate prediction of the S11 and S22 parameters, especially at the highest frequencies: this is an important feature of the method in order to design the optimal matching for the amplifier. In fact, two matching networks were designed at 14GHz on the basis of the predicted amplifier behavior provided by the proposed method and by the standard library simulations. Then the two networks were combined with the S-parameter amplifier measurements, obtained by an HP8510 using a TRL calibration and by de-embedding from GSG pads effects. The results in Fig.5c and 5d show a better behavior of the input and output return loss of the amplifier designed with the method proposed here with respect to the design carried out using the standard approach.

Moreover the Maximum Available Gain (MAG) of the amplifier has been evaluated in the range 12 – 20GHz where the circuit is unconditionally stable. Fig.6 shows the comparison between measured MAG and simulations by means of the proposed method and by using the standard libraries supplied by the foundry.

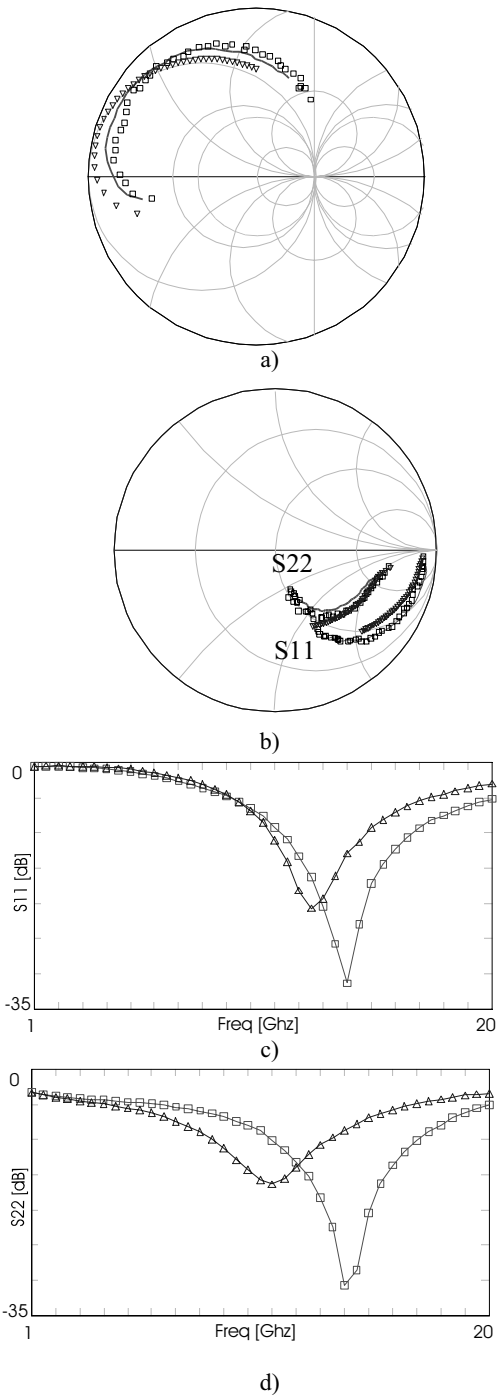

Fig. 5. a) and b): comparison of S11, S21, S22 measurements (squares), simulations with the proposed method (line) and simulations with standard libraries (triangles); c) and d) S11 and S22 for measurements combined with @14Ghz matching networks designed with the proposed method (squares) and standard libraries (triangles).

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The comparison of all the results highlights how the global modelling approach offers a better ability in predicting circuit performances and several figures of merit in the higher frequency range with respect to the traditional design approach based on the standard foundry library. The key feature of this method is the possibility of predicting the electromagnetic interaction among the different parts of the circuit in the higher frequency range.

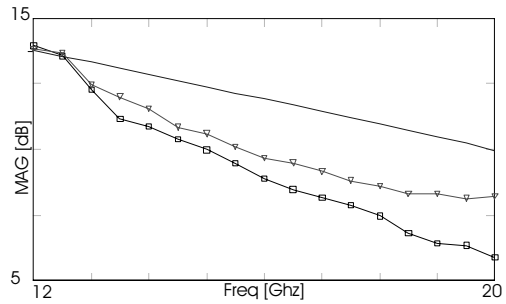

Fig. 6. Maximum Available Gain: comparison between measurements (squares) and simulations with the proposed method (triangles) and standard libraries (line).

IV. Conclusion

A novel approach to the design of highly-integrated circuits at high frequencies has been presented. The method has been used to develop a wide-band amplifier, where the ohmic electrode-sharing technology was successfully exploited.

The developed amplifier, excluding bonding pads, achieved a very small size of $0.12 \times 0.10 mm^2$, which was as small as a single-FET pattern with four gate fingers. The MMIC characterization exhibits a good agreement with performance predicted through simulations.

The adopted technique enables complex electromagnetic effects and the interactions with active devices in the design of a high-density integrated structures to be taken into account. Moreover, this modeling approach could be linked to electromagnetic optimization routines, for instance, by using the techniques proposed in [7].

Next research step will be the application of this method to more complex structures with a higher number of active devices, possibly also including passive components.

At the moment, the main method limitation is related with the capability to perform only small signal S-parameter analysis. The complete exploitation of the proposed method will be reached with the implementation of a non linear model of the active slices. The availability of such a model will allow running a complete set of simulations, including Harmonic Balance, in order to predict the non linear amplifier behavior.

The non linear extension of the proposed method, together with the scalable thermal model presented in [8] could have important applications in high power, high frequency circuits where cross talking, parasitic and thermal phenomena play an important role on the performance.

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