Low-Noise W-Band Amplifiers for Radiometer Applications Using a 70 nm Metamorphic HEMT Technology

C. Schwörer, A. Tessmann, A. Leuther, H. Massler, W. Reinert and M. Schlechtweg

Fraunhofer-Institute of Applied Solid State Physics
Tullastrasse 72, D-79108, Germany, Phone: ++49 761 5159 486

***Abstract* — W-band low-noise amplifier (LNA) MMICs have been developed using a 70 nm metamorphic HEMT (MHEMT) technology. The short gate length in combination with the high indium content of 80% in the channel lead to a maximum transconductance of 1500 ms/mm for a 2x30 µm device. This results in a transit frequency f_t of 290 GHz. Two- and three-stage amplifiers were realized in coplanar waveguide technology (CPW) and achieved a small signal gain of 13 dB and 19 dB, respectively. The noise figure at room temperature of both LNAs was below 3 dB. The on-wafer measured output power at the $P_{-1\,dB}$ compression point was 5 dBm. A modification of the three stage LNA showed a noise figure of 2.5 dB, with a small signal gain of 15 dB at 94 GHz.**

I. Introduction

Up to now radiometric sensors were commonly used in the area of radio astronomy. Because of the major advantages of these sensors, such as visibility through fog, dust, fume or even clothes, and since the systems operate passively, new fields of applications are opened for military, and even civilian use. Two examples are the detection of concealed weapons (CWD) or the landing aid at airports. Low noise amplifiers with high gain are key components in remote sensing W-band radiometer front-ends, reducing the number of cascaded amplifiers which are necessary to achieve the appropriate voltage swing for the detector in the case of direct detection. Low noise figure enhances temperature resolution or helps to reduce integration time [1]. Most of the amplifiers reported on for these applications [2-4] use an indium phosphide (InP) technology. Recently, metamorphic technologies have emerged [5], enabling larger substrate size and superior wafer handling, which finally allows for lower fabrication cost of the complete sensor systems.

II. Technology

The employed metamorphic HEMT structures are grown on semi-insulating 4" GaAs substrates. The metamorphic buffer layer consists of a linear

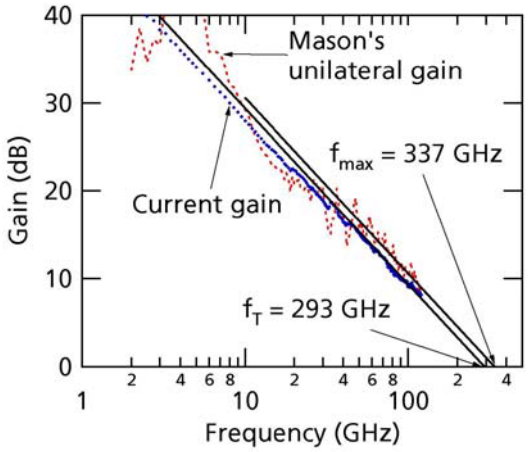

Fig. 1. Current gain and Mason's unilateral gain for a 2 x 30 µm MHEMT with extrapolated f_t and f_{max}.

$In_xAl_yGa_{1-x}As$ (x = 0 ➔ 0,52) transition, that finally yields the InP lattice constant. The layer structure comprises a composite channel consisting of an 80 % In main channel for high carrier velocity. Furthermore a 53 % indium content sub-channel was introduced, which helps to reduce impact ionization and thus improves the breakdown behavior. The on-state breakdown voltage achieved with the described layer structure is about 1.7 V and the off-state breakdown is about 2.7 V. E-beam lithography with a three layer PMMA resist was used to pattern the T-shaped gate with a final foot print of 70 nm only. The Ti-Pt-Au gates are passivated with 250 nm CVD silicon nitride. The active device area was defined using a wet etched mesa. Using this device technology a maximum extrinsic transconductance of 1500 mS/mm was reached, with an extrinsic f_t of 293 GHz and an f_{max} of 337 GHz for a 2x30 µm device as displayed in Fig. 1. Additionally, life time tests in air were performed, yielding an MTTF of 10^6 hours at a channel temperature of 125 °C. More details on our metamorphic HEMT technology can be found in [6].

III. Circuit Design

It was the goal to design low-noise amplifier circuits (LNAs) in the W-band, with an emphasis on the 94 GHz range. The FET geometry chosen was a 4x15 µm device giving the best compromise for gain and noise behavior. The starting point for the design was the small signal equivalent circuit which was extracted using S-parameter measurements between 0.25 and 120 GHz. This equivalent circuit showed a maximum extrinsic transconductance of 2100 mS/mm with an associated drain current of 450 mA/mm at a drain voltage of 0.8V. To model the noise behavior of the active device the Pospieszalski model [7] was used. This approach uses an equivalent noise temperature associated with the resistances R_i and R_{ds} of the equivalent circuit. The model was mathematically validated by [8] and [9] for the case that the gate current at the specific bias point of the device remains negligible. Due to the lack of noise parameter measurements at W-band frequencies, the gate noise temperature was set to ambient temperature (300 K), while the drain noise temperature was estimated to be 600 K. During the design phase it turned out, that the absolute value of the noise temperature in the gate and the drain path did not affect the position of the minimum noise figure in frequency. Instead, the noise figure was only shifted in its absolute level.

Two- and three-stage LNAs were designed, using our coplanar element library [10], with a ground-to-ground spacing of 50 µm. For both amplifiers the first stage was designed using inductive source lines, to optimize for low noise operation and good input matching. Additionally the three-stage LNA had its second stage provided with short transmission lines in the source path, as depicted in the schematic diagram in Fig. 2.

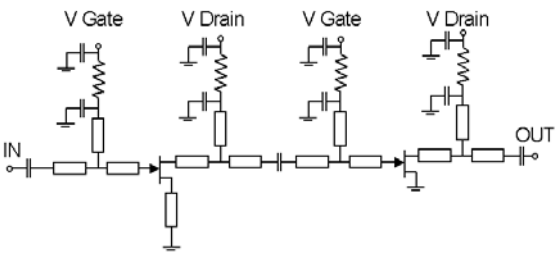

Fig. 2. Schematic diagram of the two-stage W-band low-noise amplifier.

In contrast to the input stages, the last stage was matched for high gain. Low frequency stability was ensured by using a Π-type C-R-C low pass filter to block the gate and drain bias lines from the influence of the off-chip circuitry. The chip-size for the amplifier circuits was 1x2 mm^2 and 1x3 mm^2, respectively. A picture of the two- and three-stage MMICs is shown in Fig. 3 and 4.

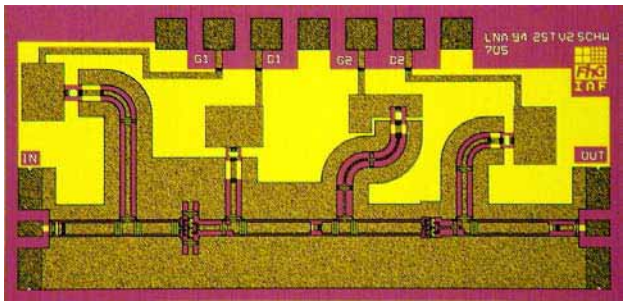

Fig. 3. Chip photograph of the two-stage LNA. The chip size is 1 x 2 mm².

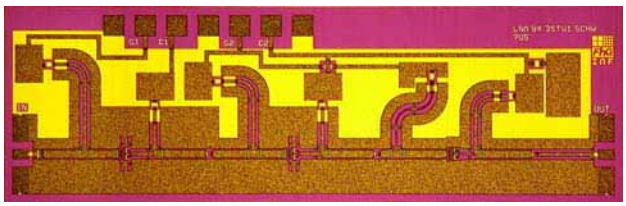

Fig. 4. Chip photograph of the three-stage LNA. The chip size is 1 x 3 mm².

IV. Experimental Results

Figures 5 and 6 show the comparison between simulated and measured S-parameters for the two- and three-stage LNA. At the higher end of the frequency band the measurements show, that gain and matching were shifted approximately by 5 GHz to lower frequencies.

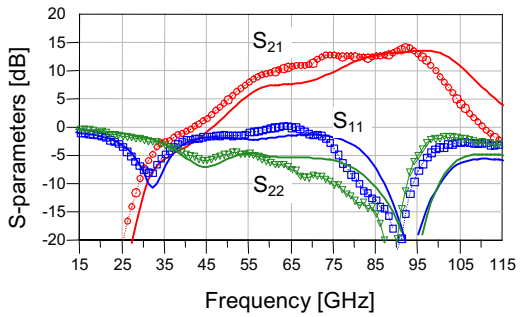

Fig. 5. Simulated (-) and measured (-∇-) S-parameters of the two-stage LNA.

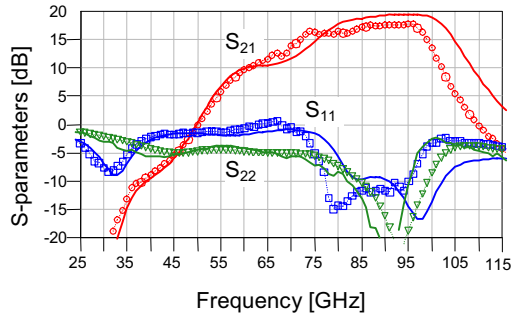

Fig. 6. Simulated (-) and measured (-∇-) S-parameters of the three-stage LNA.

Re-simulations showed that this effect could be described by a slight shift in the reference planes of the FET model. The gain level was in the order of 13 dB for the two-stage and 19 dB for the three-stage amplifier as predicted by the simulation. The noise figure of the circuits was measured using a waveguide setup between 75 and 110 GHz where both noise figure and scalar gain measurements were performed. The test bench was carefully calibrated by a "hot-cold" calibration, using an absorber that could be heated, or cooled with liquid nitrogen. To find out the optimum bias point for low-noise operation, the drain voltage and current were tuned as shown in Fig. 7. Noise figures achieved were 3 dB or slightly better up to 94 GHz for both amplifiers. The optimum current density for low-noise operation was found to be in the order of 200 mA/mm. The optimum voltage applied to the circuit was 1 V, leading to 0.8 V at the drain of each FET due to the voltage drop across the biasing resistors.

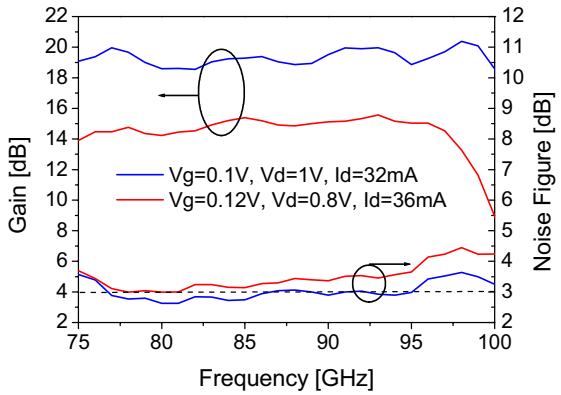

Fig. 7. Noise-figure and gain measurement for the three-stage LNA at two different bias conditions.

A modification of the three stage LNA, where only the first stage was changed to improve the noise behaviour was also characterized. This MMIC showed an improvement in noise figure by nearly 0.5 dB in the frequency band from 80 to 100 GHz compared to the previous version. One drawback of this modification was that the gain had a high frequency roll-off of approximately 0.4 dB/GHz. The scalar gain and noise measurement for this chip is shown in Fig. 8, demonstrating a gain of 15.5 dB at 94 GHz and an average room temperature noise figure of 2.5 dB.

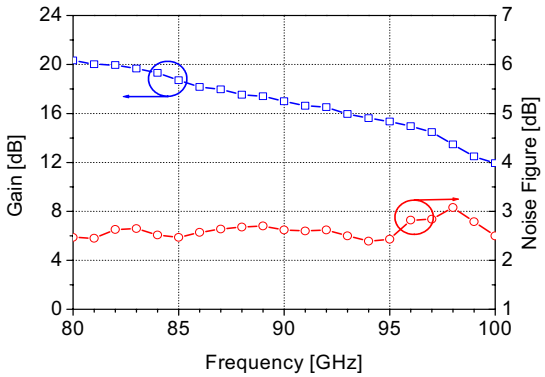

Fig. 8. Noise-figure and gain measurement of the modified three-stage LNA.

A wafer mapping of the small signal gain was performed over all 35 cells of a 4" wafer, each cell containing one two- and three-stage LNA among other circuits. The gain distribution is displayed in Fig. 9 for both MMICs indicating high uniformity across the entire wafer. The circuit yield for both circuits was exceeding 75% with 13 dB and 19 dB minimum gain as the performance criteria, respectively.

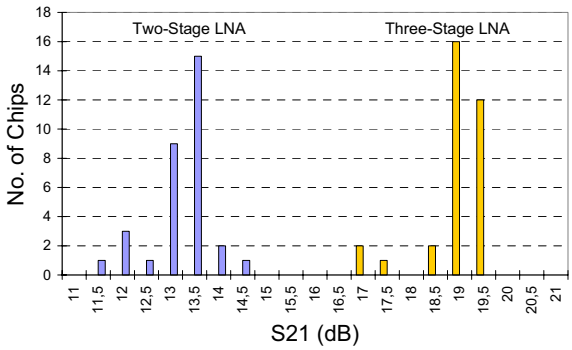

Fig. 9. Gain distribution for two-stage and three-stage LNA over one wafer.

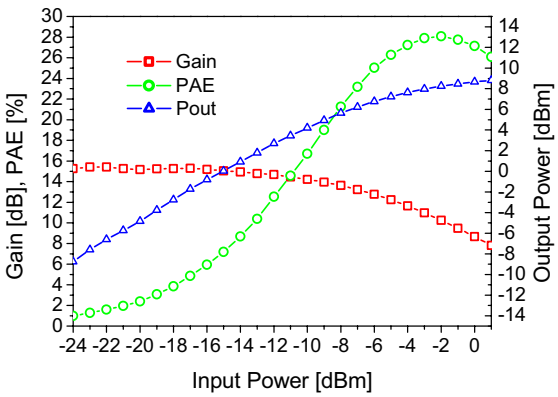

Fig. 10. Measured gain compression behavior of three-stage LNA with a $P_{out\text{-}1\ dB}$ of 5 dBm.

Radiometers which employ the method of direct detection have typically an overall gain of 60 dB before the signal is fed to the detector diode. To get the correct value of the detected power, one has to ensure that the

last amplifier stages operate in a linear mode. This problem is even emphasized if a large RF bandwidth is used to keep the integration time short. Thus, we measured the saturation behavior of the three-stage LNA at 94 GHz as shown in Fig. 8. The bias conditions for the amplifier were a drain-voltage of 1.5 V and a gate-voltage of –0.1 V resulting in a 24 mA quiescent drain current. compared to the low noise measurement, this is below the maximum transconductance, which leads to 3 dB lower gain of the amplifier. At the compression point an output power of about 5 dBm was achieved with an input power of –10 dBm. It is remarkable that the power added efficiency at $P_{-1\,dB}$ was 18 % and the maximum PAE was as high as 28 %.

VI. Conclusion

Low noise amplifiers using an advanced 70 nm metamorphic HEMT technology on 4'' GaAs substrates were presented. The first iterations of the two- and three-stage amplifiers showed 13 and 19 dB gain and a noise figure of about 3 dB in the frequency range from 80 to 100 GHz for both amplifiers. A second iteration of the three-stage LNA leads to an improvement of the noise figure to 2.5 dB. The $P_{-1\,dB}$ compression point at the output of the three-stage LNA was 5 dBm. Both, circuit performance and yield demonstrate the excellent potential of metamorphic HEMT technology to compete with state-of-the-art InP technologies [11], combining all the advantages of using GaAs substrates.

Acknowledgement

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