A Compact, Semi-Physically Based Model Predicts Accurate Power And Linearity of Power InGaP HBTs

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ABSTRACT

A compact and robust InGaP-GaAs HBT model has been developed for accurate large-signal and linearity simulations. In addition to self-heating, the model takes into account the non-quasi-static charge effects, which include collector mobile charge effects, collector transit time effects, and other dynamic charge effects. The new model, in contrast to conventional HBT models, predicts very well the large gain expansion at class AB operation and also the distortion, such as IP3, at various harmonic load conditions. The model is semi-physically based and, therefore, can be used to assess the effects of physical parameters on linearity, such as collector doping.

INTRODUCTION

In the past years, InGaP-GaAs HBT power amplifiers have been attracting a great interest for ultra-wide band wireless communications due to their high linearity and single polarity bias. To accurately predict the power and distortion performance and to optimise the device structure, an accurate and physically based HBT model is highly desirable. Among others, the IP3 or two-tone behaviour presents a most severe challenge to engineers, since it requires a higher order fitting to device IV as well as QV characteristics.

A number of HBT models have been proposed with emphasis on self-heating effects [1-4]. Some of them have taken into account non-quasi-static charge effects [3,4]. The trans-capacitance of the base-collector junction has been shown to have higher-order effects on HBT performance, namely linearity and distortion. L. H. Camnitz proposed a physically based model that includes a unified collector charge term that was verified only by the device's frequency-response behavior [5]. A carefully extracted Gummel-Poon (GP) based HBT model combined with self-heating is, in most cases, sufficient to fit the dc as well as the small-signal response at various forward-operation biases. The GP-based classic model, however, fails to generate accurate large-signal power response at certain bias regions and is unable to accurately predict linearity performance. Using various models, doping effects on linearity have been studied by several other groups. [6,7]

In this paper we present a compact, comprehensive, and semi-physically-based HBT model that can accurately predict power performance and distortion at various biases, fundamental and harmonic loading conditions, and envelop frequency loading conditions. Collector and emitter layer doping effects on gain flatness and linearity are also simulated to assess these device structure effects. The simulation has been compared to the measured results.

MODEL FORMULATION

Figure 1 shows the schematic of the model. It is composed a conventional GP BJT model, a self-heating thermal circuit, and a collector-charge element. To add the self-heating effects and to modify the collector charge expressions, Bf and Cbco have been disabled in the GP part of the model, and their associated parts are moved outside the GP transistor. The self-heating caused temperature rise is modeled by a thermal-subcircuit, and two nonlinear feed-back circuits, as shown in Figure 1, are used to model the decrease in Vbi of the junctions and the decrease of current gain with temperature.

Given a conventional GP model with a collector charge term $Q_{co}(V_{bc},C_{bco}(N_c))$, where C_{bco} is the zero bias capacitance, the collector charge is expressed as

$$Q_{bc}= \int I_c(\, t-\tau_c(V_{bc}\, , I_c))dt + Q_c(V_{bc}\, , I_c), \tag{1}$$

$$\tau_c(V_{bc}\, , I_c)=W(V_{bc}\, , I_c)/V_{sat}, \tag{2}$$

and

$$Q_c(V_{bc}\, , I_c)= Q_{co}(V_{bc}\, , C_{bco}(1- I_c/ I_{crit})^{1-mc}), \tag{3}$$

where $V_{sat} = 10^7$ cm/s and $I_{crit} = qA_E\, N_c\, V_{sat}$ with A_E being the emitter area. W, the width of collector depletion region, is a function of V_{bc} and I_c and can be expressed as

$$W= (2(V_{jco}-V_{bc}\,)\varepsilon/(qN_c - I_c/A_E V_{sat}))^{0.5}. \tag{4}$$

When punch-through occurs at a certain Vbc, W is set to equal to the Lc, the collector epitaxial layer thickness. It was found that the Kirk effect for III-V compound-semiconductor HBTs does not significantly affect the current, but will increase the time constant TF. The Kirk effect threshold, ITF, in the GP model, therefore, is expressed as

$$ITF=qA_E\, N_c\, V_{sat}(1+2*\varepsilon\,(V_{jco}-V_{bc}\,)/(\,qN_cA_EV_{sat})). \qquad (5)$$

Normally, the emitter of an InGaP-GaAs HBT has two layers: one InGaP layer and one highly doped GaAs layer. Its capacitance-voltage characteristics manifest two regions of distinct behaviour. The Cbe(Vbe) is modified as follows.

$$C_{be}=C_{beo}/(1-V_{be}/V_{je1})^{m1} \quad if\ V_{be}<V_t \qquad (6a)$$

$$C_{be}\ =C_{be1}/(1-V_{be}/V_{je2})^{m2} \quad if\ V_{be}>=V_t \qquad (6b)$$

Based on device physics Cbe1 can be written as

$$C_{be1}=A_E*(\ qNe\ \varepsilon\,/(2V_{je2}\,))^{0.5}, \qquad (7)$$

where *Ne* is the doping of emitter layer next to the base. Matching the values in (6a) and (6b) at Vt gives

$$C_{be1}=C_{beo}(1-V_t/V_{je2})^{m2}\,/(1-V_t/V_{je1})^{m1}. \qquad (8)$$

Vt can be determined by the critical point where the InGaP emitter layer is fully depleted and the high-doped emitter layer is not depleted. The two section Cbe(Vbe) characteristics allow one to tune the doping of InGaP and GaAs emitter layers independently.

The model modifications involve several nonlinear functions, and, in most simulators, there is no way to modify the GP model. Therefore, the whole model is realised with a symbolically defined nonlinear device in Agilent's Advanced Design System.

MODEL EXTRACTION AND VERIFICATION

To extract large-signal models of HBTs, dc, thermal and S-parameter characterization have been utilized. A conventional GP model in conjunction with the self-heating circuit is first used to fit Ic-Vc and Vbe-Vc curves. The capacitance-voltage dependencies of both junctions are extracted at Vbe<1.2 V and Vbc<=1.0 V or cut-off conditions, and the Cbe(Vbe) fitting is shown in Figure 2. The forward and collector transit times as a function of Vcb and Ic is extracted from the S-parameters at lower-current active biases.

At the higher currents, the small-signal circuit involves two trans-capacitances and the extraction becomes more difficult. We adopted an approach based on device physics, utilizing Equations (2) to (5).

The transistors have emitter area of 240 and 960 um^2 and have series resistors at the base and emitter for electrical and thermal stability. The thermal resistance, Rth, was measured and fitted by the formula, Rth= $46639x(A_{cb})^{-0.7463}$. The self-heating effect on the built-in voltage is modeled by $\delta V=-0.0012*\delta T*exp(\delta T/To)$, and its effect on current gain is expressed by a nonlinear term $\delta\beta=-0.014*\delta T/(To*nf*Vt)*exp(\delta T/To)$. The dc and parasitic related parameters for a unit cell of 240 um^2 are: Iso=1.52e-24, Nf=Nr=1.008, Bf=133.0, Ise=1.53e-22, Ne=1.285, Isc=1.2e-14, Nc=1.88, Br=0.4, xcjc=0.63, Re=0.353, Rbi=0.55, Rbx=1.046, and Rc=1.144.

The charge related parameters are Cjc=0.205pF, Vjc=1.23, mc=0.55, Cbeo=0.541pF, Vje1=1.14, m1=0.0964, Cbe1=0.356pF, Vje2=1.4 m2=0.5, xtf=0.7, vtf=-5, and Tr=50ps. The time constants at Vc=3V and Ico=10mA are extracted as Tfo=0.5ps and Tco=4.5ps.

The model was verified by comparing the simulated DC curves and S-parameters at several lower current biases over the frequency range of 0.2 to 15.2 GHz. The fitting was excellent, and it is found that there is no significant difference between the GP model combined with self-heating and the new model. However, when biased at class AB and presented with certain loading conditions, the device shows a remarkable gain expansion that the GP model fails to fit in spite of attempts at retuning the model parameters. On the other hand, the new model accurately predicts the power gain expansion and power added efficiency. Figure 3 shows a comparison of the measured data, the GP-self-heating model, and our new model. The device has an emitter area 960 um^2. It was biased at Vc=3.2 V and Ico=16 mA. The source side is tuned at $\Gamma_S=0.62\angle 150$. The load at the 900 MHz fundamental is $\Gamma_1=0.6\angle 154.4$. At the second harmonic the load is $\Gamma_2=0.73\angle -77.8$, and at the third harmonic it is $\Gamma_3=0.44\angle -78.8$. At this harmonic loading condition, the device shows its best PAE.

In order to verify the physical model, we measured and simulated power gain for devices with different collector dopings. Again, the device area is 960 um^2. Two devices were measured: one with a collector doping of $2x10^{16}\ cm^{-3}$ and the other with $1x10^{16}\ cm^{-3}$. The devices were biased at Vc=3.2 V and a quiescent current of Ico=10 mA. Source and load-states are very close to those give above. In our semi-physically based model, it is straightforward to simulate the collector doping effects without the need to extract individual models. Figure 4 shows modeled and measured power gain verses input power. The dotted line and triangle symbols show the modeled and measured data for the lower doped device, and the solid-line and square symbols are for the higher-doped device. Good agreement between the measurement and simulation can be seen.

LINEARITY MODELING FOR DEVICE OPTIMIZATION

The third order intermodulation, IM3 is directly related to the harmonic loads. To further verify the model, simulation of harmonic power at several harmonic terminations is performed and compared to the measured data. Figure 5 show a typical case where the source is tuned at Γ_S=0.57$\angle$145, and the load reflection coefficients of the fundamental, 2nd and 3rd harmonics are Γ_1 =0.35$\angle$165, Γ_2 =0.71$\angle$-22.4, and Γ_3=0.55$\angle$3.1, respectively. The device has a emitter area of 960 um^2. The agreement of the simulation and the measurement, as shown in Figure 5 is impressive.

To find out an optimum HBT structure that maximizes IP3, we first measured the IP3 dependence of HBT structures under various bias and loading conditions. Two-tone measurements were performed with an ATN load-pull system. The two tones are at 0.9 GHz and 0.901 GHz with a beat frequency of 1 MHz. Simulation of the two-tone power performance was performed at a selected loading condition that shows better two-tone results. Figure 6 compares modeled and measured two-tone results. The device again has an emitter area 960 um^2. It was biased at Vc=3.2 V and Ico=42 mA. The source side is tuned at Γ_S =0.52$\angle$165.7, and the load, numbered as 211040, has reflection coefficients of Γ_1 =0.16$\angle$-14.2, Γ_2 =0.51$\angle$36.8, and Γ_3 =0.59$\angle$-112.5. At this particular harmonic loading condition, the device shows better IP3. The 2nd harmonic loading is close to that predicted in literature [8].

It is seen that there is good agreement between measurement and simulation at the lower power region. Under high power drive, the distortion is highly dependent on the biasing circuit that affects the impedance at the beat frequency. In general, higher inductance decreases distortion increasing IP3 but slightly lowers the output power. Given that the load impedance at the beat frequency is unknown in the measurement system, the model verification in terms two-tone measurements is fairly satisfactory.

To gain an insight into the major factors influencing distortion and to optimise the device structure, we have measured and simulated the distortion dependence on different device emitter and collector structures. It has been shown that the emitter capacitance characteristics or the emitter layer doping have only a minor effect on distortion. On the other hand, the collector structure has a remarkable effect on the distortion. Simulation is performed for an HBT at the load state 211040 with Vc=3.2V and Ico=0.4A. Figure 7 is a 2D-surface plot showing the IP3 as function of Nc and Lc. The input power is -10 dBm. It is seen that optimum linearity can be achieved in two extreme regions. One is the punch-through region, and the other is a highly doped and thick epi-layer region. The difference between best case and worst case can be as high as 12 dBm. The simulation results are experimentally supported by other publication.[9]

CONCLUSIONS

An accurate, compact, semi-physically based HBT model is developed. In addition to conventional prediction of the dc curves and S-parameters, the model successfully predicts the power and distortion (that is inter-modulation) performance at harmonic tuning conditions. The model is expected to be very useful for power amplifier design due to its accuracy and computational-efficiency. The model is analytical and semi-physically based and, accordingly, can be applied to device structure optimization without the need of extracting and comparing experimentally individual models of different structures.

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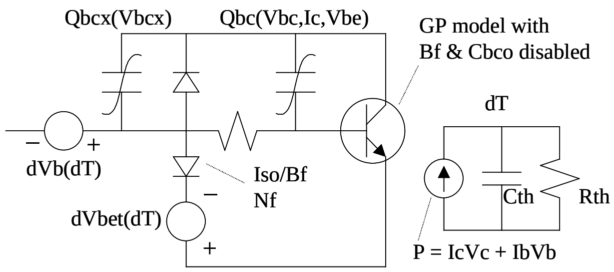

Figure 1. Schematic of intrinsic HBT model consisting of a GP HBT model, thermal circuit, two feedback sources and modified BC charge

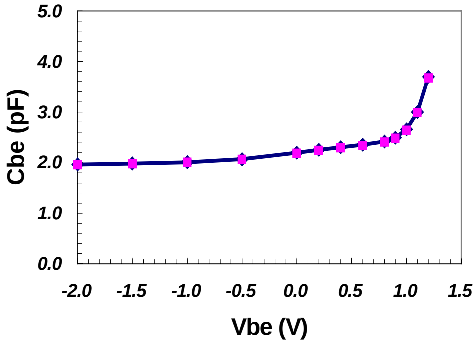

Figure 2. Fitted (line) and measured (symbol) BE-capacitance characteristics. The emitter area is 960 um^2

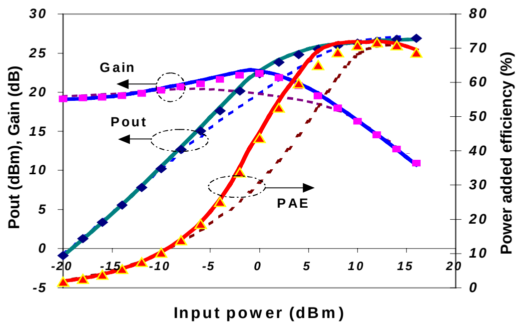

Figure 3. Modeled with new model (solid-line) and with GP model (dotted line) vs. measured (symbol) power performance. Ae = 960 um^2. Vc=3.2 V. Ico=16mA.

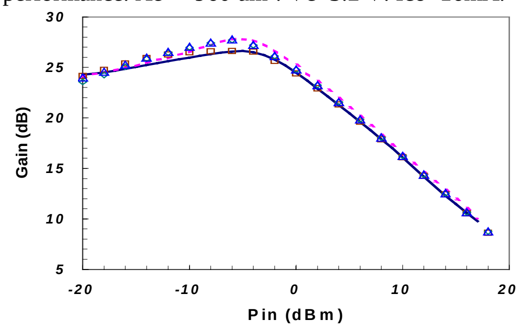

Figure 4. Modeled (line) vs measured (symbol) power gain verses input power. F=0.9GHz. Vc=3.2V., Ico=10mA. Solid-line and square: Nc=$2x10^{16}$ $cm^{-3.}$ Dotted-line and triangle: Nc=$1x10^{16}$ cm^{-3}

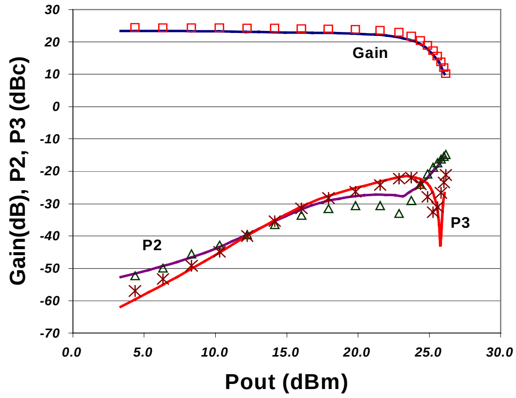

Figure 5. Modeled (line) verses measured (symbol) power gain, 2^{nd} and 3^{rd} harmonic power as function of input power with harmonic tuning. F=0.9GHz, Vc=3.2 V and Ico=40 mA.

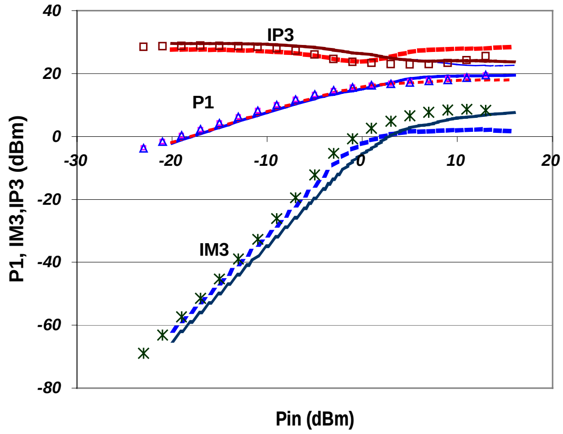

Figure 6. Modeled (line) vs. measured (symbol) one-tone-power (P1), the 3^{rd} order intermodulation (IM3), and the third order intercept point (IP3) as function of input power. F=0.9GHz, Vc=3.2V, Ico=40 mA, harmonic tuning, load at fundamental 0.16∠-14.2. The dotted line and solid line shows results for different beat frequency impedances.

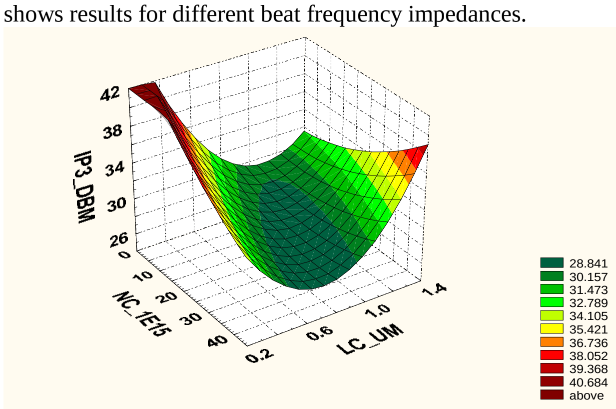

Figure 7. Modeled 2-D plot of IP3 verses collector doping, Nc and epi-layer thickness, Lc.