L-Band MMICs for Space-based SAR system

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The design and performance of an L-Band GaAs chip-set is presented. The chip-set consists of a 6-bit attenuator circuit, a Low-Noise Amplifier (LNA) and a Multi Function Chip that is the combination of a 6-bit attenuator and 6-bit Phase shifter circuit. The chip-set is developed for the pre-flight engineering T/R (Transmit and Receive) modules currently in development with Astrium in a space-based SAR (Synthetic Aperture Radar) system. The MMICs are realised in the 0.25μm PHEMT (PH25) technology of UMS. Only one iteration was needed for the MMICs in order to be fully compliant with the specifications.

INTRODUCTION

Today there is a increasing demand for small T/R modules, with low power consumption and low cost. In an effort to meet these difficult requirements MMICs are increasingly being used, even at L-band.

In this paper we describe the following MMICs; A Low Noise Amplifier (LNA), an Attenuator and a Multi Function Chip (MFC) which form part of a L-Band T/R module.

The design goal for the MFC is to replace the separate Phase and Attenuator chips with a single MMIC. Further, this MMIC is an excellent candidate for the common leg of a T/R module.

For the specific application, stringent specific design constraints exist. These include, size, input/output pins, functionality and performance.

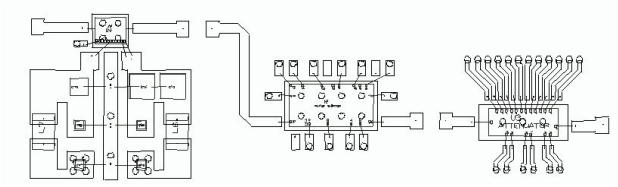

Figure 1: MMIC line-up in L-SAR T/R module

LNA DESIGN AND MEASUREMENT

The LNA has a number of specific features:
- High gain (>23 dB)
- Input protection against RF input levels of 20dBm
- Active on-chip bias circuitry

To realise 23 dB of gain, two stages of amplification are required. However using the PH25 UMS process a gain of 28 dB is achievable, using only 2 stages. At this gain level, which has been demonstrated by measurement, the number of LNAs in the system can be reduced from 3 to 2, thus reducing the overall DC power consumption of the T/R module.

A specification of +20dBm continuous input power is required when the LNA is turned off, which is known as “damage level” (T/R module is in transmit mode). Since the PH25 process does not allow for this input power handling capability some form of protection circuitry is required.

Without any kind of protection circuitry the maximum RF voltage swing on the gate of the input FET would be exceeded for powers levels in excess of +6 dBm. To solve this implementations of several “limiting types” of circuits were investigated. The best solution we found to meet the specification was the addition of a FET (6-fingers, 240um gate width) in parallel, effectively reflecting all the incident power at the amplifier input when turned on.

The increase in Noise Figure of the LNA due to the addition of the protection circuitry is less than 0.05dB. A separate bond-pad was added to control the FET. The levels used for switching are 0/-5V and could be connected directly to the –5V supply of the amplifier.

Active on-chip bias circuits are implemented for the following reasons:

- to reduce the impact of process variations on the performance of the LNA
- to minimise the effect of bias levels
- to minimise the uncertainty in the DC operating condition of the FET.

The schematic of the bias circuitry is shown in figure 2

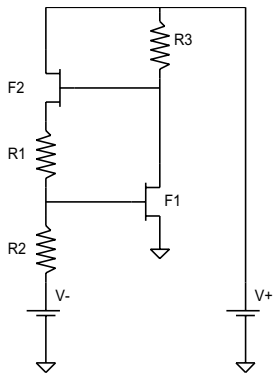

Figure 2: Active bias of the LNA stages.

The negative power supply voltage together with R2 form a current source feeding R1, giving a reference voltage at the source of F2. The gate of F2 "measures" the drain-voltage of F1 and compares it with the reference voltage on its source. The error current drives the gate of F1, effectively creating a closed-loop circuit.

Series feedback using a source inductor is used to enable a simultaneous match for low noise and good input matching. For frequencies far below the transition frequency the input impedance of the FET is high, therefore a MIM capacitor was placed in parallel to the gate to improve the matching. Using this additional capacitor reduces the effect of the PH25 process spread on the input matching, thus enabling the design to be much less sensitive to process variations.

Figure 3 shows a photograph of the realised LNA which measures 1.6×1.4 mm².

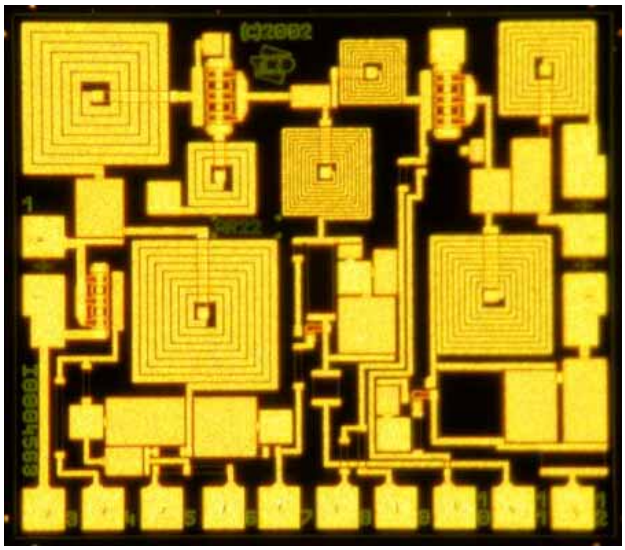

Figure 3: Photograph of the LNA

A total of 1272 LNAs have been measured on three different wafers (1r003, 2r004 and 5r008). A direct comparison between the simulations and measured performances is shown in figures 4 through 6. For each wafer a separate curve is added. Each measured curve represents the average performance of all LNAs on one wafer that passed the DC, RF and visual tests. The measured insertion gain is higher than 28 dB in the band of interest. Note that wafer to wafer variation of all measured parameters is very small.

The difference in shape between the simulated and measured gain curve is due to the large inductances of the DC biasing needles used during the on-wafer measurements. With the correct decoupling of the MMIC in the application, the gain shape will be as was initially simulated.

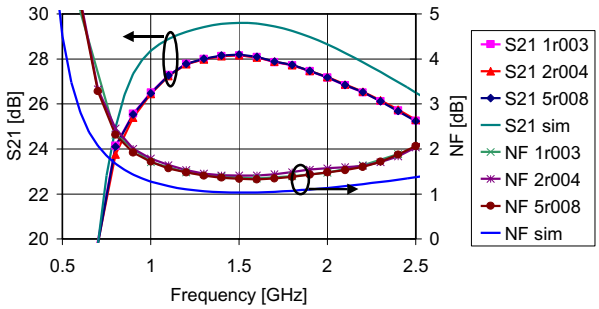

Figure 4: Measured mean Insertion gain and noise figure for 3 wafers

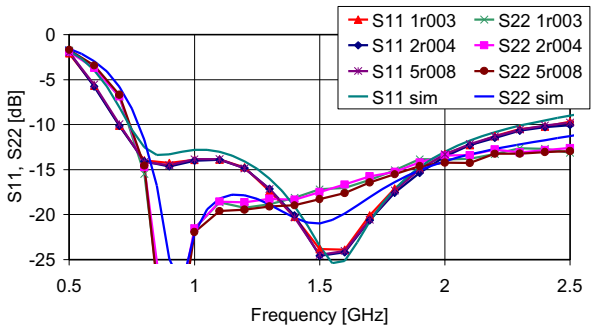

Figure 5: Measured mean input and output return loss.

The measured 1 dB compression point is in close agreement with the simulation.

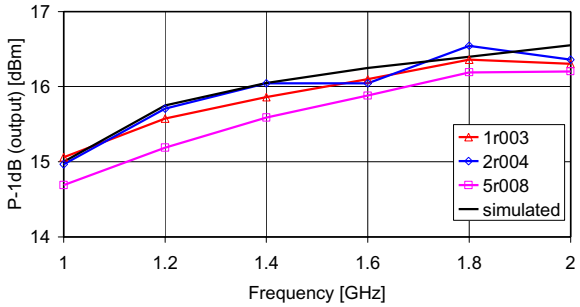

Figure 6: Measured mean 1-dB compression point.

ATTENUATOR DESIGN AND MEASUREMENT

A large number of design issues need to be considered to design the 6-bit digitally controlled attenuator:

- operation frequency up to X-band while maintaining good RF performance
- less than 4 degrees of insertion phase variation when switching from one attenuation state to the other
- less than 50 nsec (goal 5nsec) switching time
- less than 5 dB insertion loss at 8 GHz
- an input 1-dB compression point of at least 13dBm
- form fit, pin position and pin functionality compatible with the existing attenuator

To realise the above requirements the attenuator chip was built out of 7 sections as shown in figure 7.

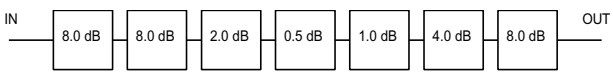

Figure 7: Block diagram of the attenuator.

Depending on the attenuation required by each of the sections a bridged T-type network or a bridged PI-type network was chosen. An exception was made for the 0.5 dB section. This section uses the difference in series resistance of 2 FETs to realise the 0.5 dB step.

In a trade off between insertion loss, phase and amplitude accuracy, it was found that the bridged T-sections are preferred for the smaller bits up to 4 dB. For higher attenuation sections the bridged PI-section was found to be better. Since the maximum isolation that can be achieved by one FET is limited and the accuracy of the attenuation sections more or less rely on the isolation, the 8 and 16 dB sections were more difficult to realise. To realise the 16 dB section it was found that the best performance was obtained by using two separate 8 dB sections. The capacitors in parallel to the resistors in the 8 dB section improve the phase accuracy when switching from one state to the other.

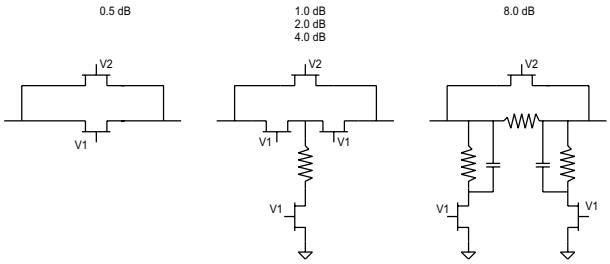

Figure 8: Attenuator sections used.

The insertion loss specification was used to determine the minimum size of this FET. Process variation and metallisation losses were also considered. For a low insertion loss a large FET is required. However, this is in contradiction with the requirement that a small equivalent capacitance is required to achieve good phase accuracy.

The resistance values to obtain the required step sizes were calculated from standard textbook equations. The values are compensated for the equivalent resistances of the series FETs in the parallel branches. These FETs also improve the attenuator performance.

High value resistors are used to isolate the RF circuitry from the DC control circuitry connected to the bond-pads in the module. These high value resistors in combination with the FET capacitance (C_{gs}, C_{gd} and C_{ds}) determine the switching speed. The chosen value was a trade off between isolation, switching speed, power handling capability and digital control current (max 100µA per section).

Figure 9 shows a photograph of the realised chip, which measures 3.45×1.4 mm². A total of 1214 attenuators have been measured on three different wafers (1r003, 2r004 and 5r008).

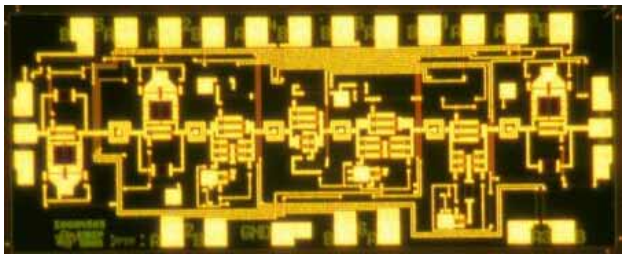

Figure 9: Photograph of the attenuator.

The attenuation error is shown in Figure 10. Each curve represents the average of all attenuators that passed the DC, RF and visual tests. The relatively large error at higher attenuation states is due to step-size of the 8 dB sections that is too large. A modification of this section would reduce the error to the simulated 0.4dB at 8GHz.

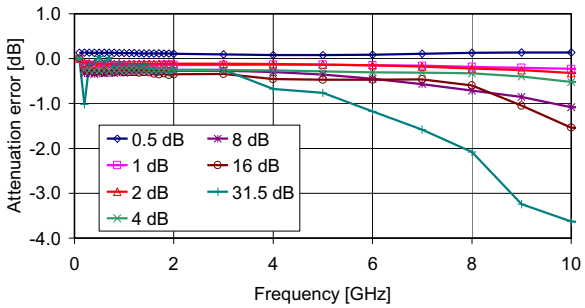

Figure 10: Mean attenuation error versus frequency.

The measured insertion loss is given for the three wafers (figure 11). Each curve represents the average of the insertion loss of all "known-good" attenuators on that wafer. Note that the insertion loss is less than 5 dB up to 10 GHz for most of the samples and that at 8 GHz the insertion loss is considerably lower than simulated.

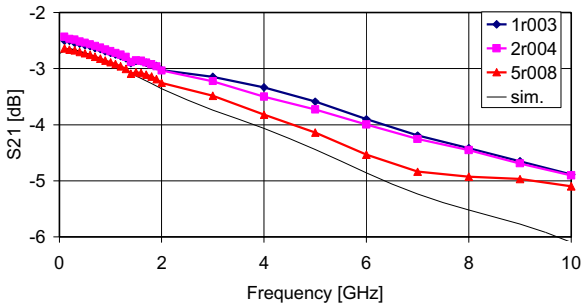

Figure 11: Measured Insertion Loss in the reference state for three wafers.

The measured and simulated 1 dB compression point is shown in figure 12. The measurement stops at the maximum rated input power of 18 dBm. The actual compression point of setting 8 dB and 16 dB is higher than 18 dBm.

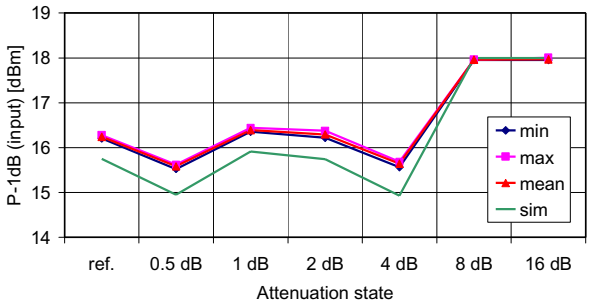

Figure 12: Measured input compression point at 1.2 GHz.

MULTI-FUNCTION CHIP

The Multi Function Chip is a combination of a 6-bit phase shifter and the attenuator chip described above.

The operational frequency is specified between 1.2 and 1.4 GHz with a maximum insertion loss of 14dB. Similar to the attenuator design it was required that the phase and amplitude variation due to state switching was minimised. Four different phase shifter topologies were used to realise the 6-bits. They are shown in figure 13.

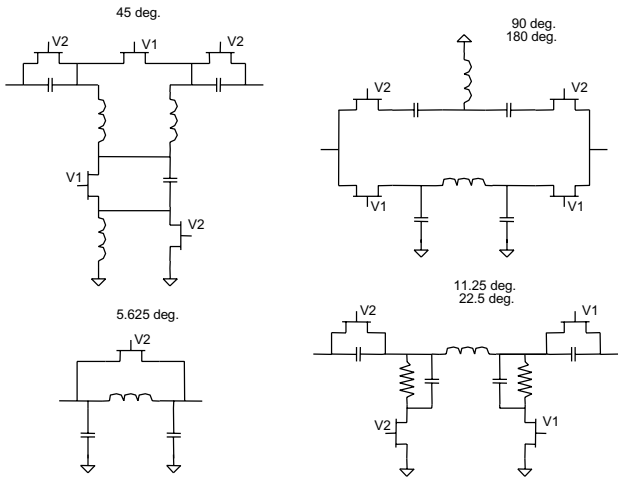

Figure 13: Circuit diagrams of the phase shifter sections.

The position of the phase shifters in the entire chain is based on the P1dB of that section. The sections with the largest P1dB are placed close to the input, thus creating the largest P1dB for the overall chip. The line-up is given in figure 14.

Although the architecture of the 5.625º section has a very limited frequency bandwidth, it was chosen because of its small size and low insertion loss.

The 11.25º and 22.5º phase shifters are implemented as a single section. With the proper bias settings the required phase shifting is achieved. The resistors in parallel to the capacitors are used to minimise the amplitude variation when switching between states. The 45º section uses a low-and high pass filter with combined inductors to save space. In the 90º and 180º sections the amplitude variation is minimised by proper selection of the FET sizes.

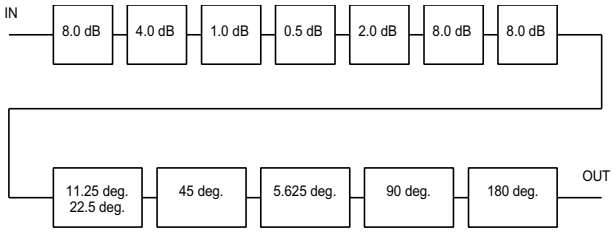

Figure 14: Block diagram of the phase shifter bits.

Figure 15 shows a photograph of the realised chip, which measures 3.45×4.2 mm².

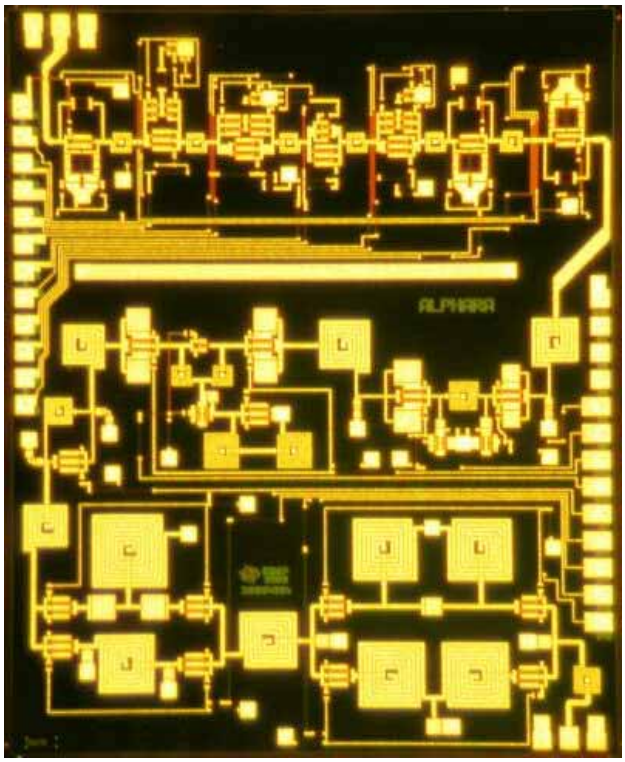

Figure 15: Photograph of the MFC.

In figure 16 the phase change versus all attenuation states is shown for a typical sample. Fortunately the largest phase change occurs for the largest attenuation states where phase change has less impact on the system performance.

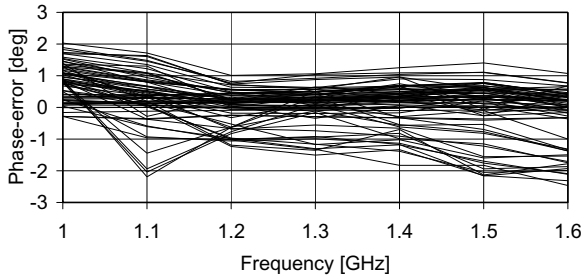

Figure 16: MFC phase error over all attenuation states for a typical sample.

In figure 17 the mean phase error for the cardinal phase states is shown along with some simulation data. It can be seen that the measured phase is less than simulated and the centre frequency has shifted upwards.

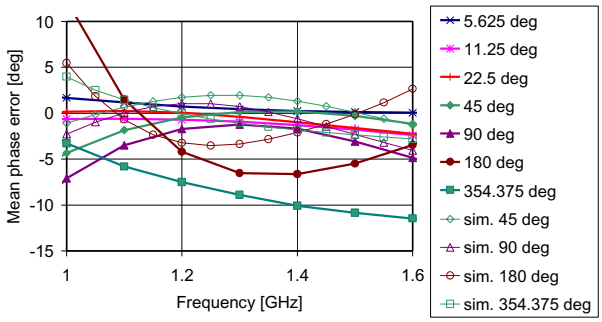

Figure 17: MFC mean phase error in cardinal phase states.

The mean attenuation error is depicted in figure 18. The simulated error is within 0.2 dB. It can be seen that the 8 dB sections used to realise states 16 and 32 have too much attenuation (identical to the attenuator MMIC).

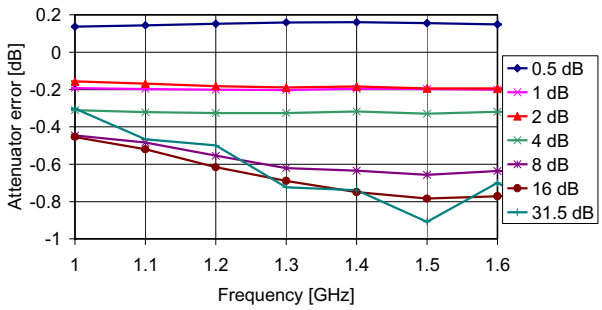

Figure 19: MFC mean attenuator error in cardinal attenuation states.

Figures 19, 20 and 21 show the S-parameters of a typical MFC for all phase states.

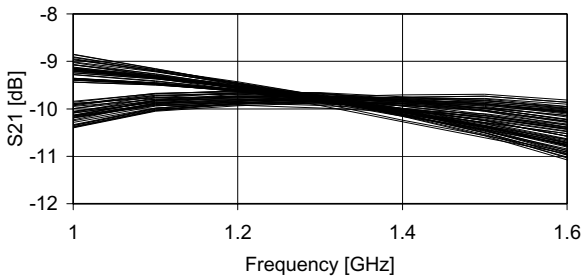

Figure 19: MFC Insertion loss over all phase states for a typical sample.

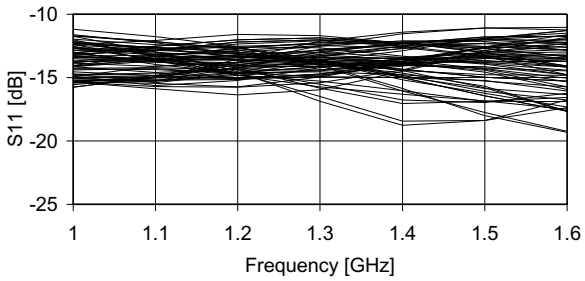

Figure 20: MFC input return loss over all phase states for a typical sample.

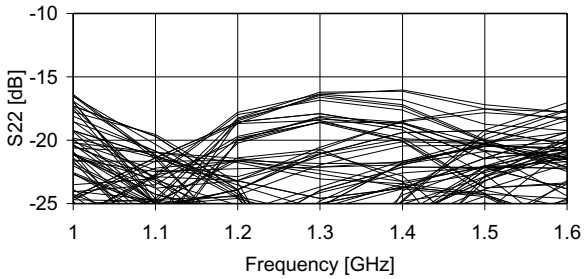

Figure 21: MFC output return loss over all phase states for a typical sample.

In figure 22 the insertion loss in the reference state is shown for all "known-good" MFCs. It can be seen that the insertion loss is 0.5 dB lower than simulated.

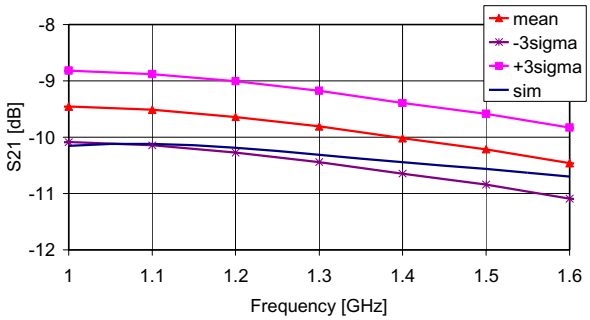

Figure 22: MFC insertion loss in reference state.

WAFER PROCESSING AND STATISTICS

The space-qualified PH25 GaAs- MMIC process of UMS is chosen for the integration of these designs. The PH25 processs enables the use of GaAs 0.25 µm gate-length pseudomorphic high-electron mobility transistors, Schottky diodes, 2 metal layers, inductors, via holes, MMIC-capacitors and metal film resistors.

Three 4 inch wafers were manufactured to obtain the required number of functional LNAs, Attenuators and Multi-function chips. A total number of 1272 LNAs, 1214 Attenuators and 150 Multi Function Chips were fully automatically tested by TNO-FEL.

Approximately 84% of the LNA dies passed the visual, DC and RF test. The yield figures for the attenuator and the MFC was 71% and 66% respectively. These global yield figures take into account all the chips of the full wafer, including the partially processed chips located at the wafer edge. The number of the good LNA and attenuator die have now been successful integrated and tested in the T/R MultiChip Modules, see figure 23.

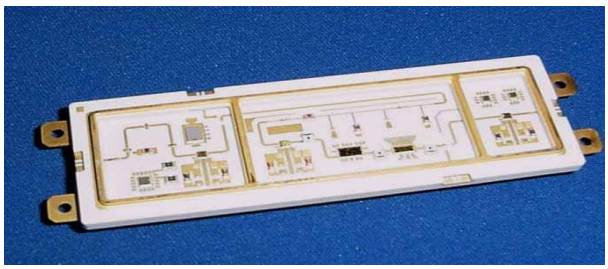

Figure 23: MCM with 3 LNAs, attenuator and control MMICs

CONCLUSION

The design and measured results of an L-Band Low-Noise Amplifier, Attenuator and Multi Function Chip are presented. These devices form a matched chip-set that can be directly applied into an L-Band T/R module.

Despite the fact that the chip layouts are very compact a first pass success was achieved. Yield figures of 84%, 71% and 66% for respectively the LNA, Attenuator and MFC were obtained.

ACKNOWLEDGEMENT

The development of the MMICs presented in this paper was performed under ESA contract.