An Integrated SiGe Dual-band Low Noise Amplifier for Bluetooth, HiperLAN and Wireless LAN Applications

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Abstract — **A bandpass low noise amplifier (LNA), which can simultaneously operate at two different frequency bands — 2.35GHz-2.6GHz and 5GHz-6GHz, is presented in this paper. The proposed dual-band LNA can be used for the Bluetooth, HiperLAN and Wireless LAN (IEEE 802.11a) communication applications, and is designed based on IBM 0.25μm SiGe BiCMOS technology, which has better performance comparing with silicon technology, while lower cost and better integration feasibility comparing with GaAs technology.**

I. INTRODUCTION

Wireless services industry has experienced a tremendous growth in the past few years [1-2]. Mobile cellular and home cordless telephones are fast becoming a part of our daily lives. The wireless local area network (WLAN) communication and home RF network are becoming popular as well. Fig. 1 illustrates the receiving band distribution of current wireless communication standards in the range of 2.4GHz-6GHz. With so many communication standards, one may consider to develop multi-functional devices, which can operate at several bands and different modes. However, traditional multi-function device is often bulky and power hungry in general, which limits the size, weight and the battery life of the wireless communication devices [3-5]. Thus, development of a single-chip multi-function RF receiver with low-cost, low-power and small form-factor characteristics is in demand [4-5].
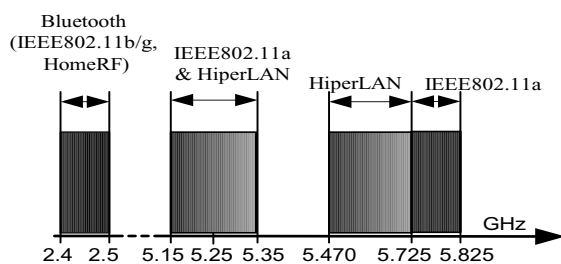

Fig. 1. Receiving band distribution of current wireless communication standards in the range of 2.4GHz-6GHz

One of the key bottlenecks for the multiple-standard communication devices is to design a single LNA that can operate at different frequency bands, since the LNA is a very important building block of a single-chip RF receiver and locates at the first stage of the receiving path.

Most of the latest LNAs reported in the literature are single-band LNAs. Currently, there are a few dual-band LNAs used for dual-band applications [6-7]. However,
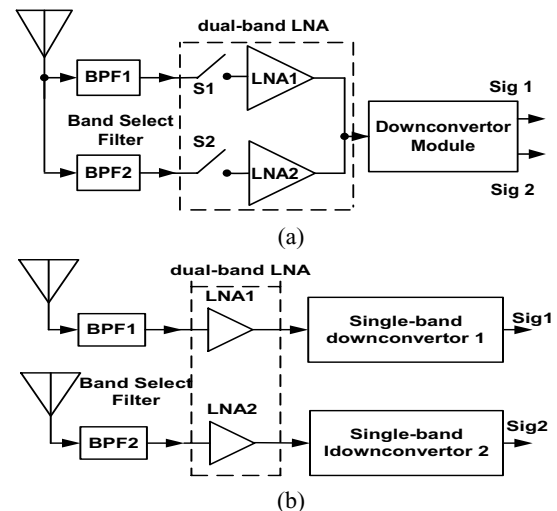

Fig. 2. Two conventional dual-band LNAs in RF receivers [6-7]

they will cause inevitable increase in the cost, footprint and power dissipation, because each LNA (illustrated in Fig. 2 (a) and (b)) uses two single-band LNAs, either one of which is selected according to the instantaneous band of operation [6], or both of which are designed to work in parallel using two separated input matching circuits and two separated resonant loads [7]. The former approach is non-concurrent while the latter consumes twice as much power.

In this paper, a dual-band bandpass LNA, which can provide simultaneous gains and matching at several frequency bands of interest, will be investigated as one of the alternatives to alleviate the above-mentioned problems.

The proposed LNA is designed to work at 2.35GHz-2.6GHz and 5GHz-6GHz for the Bluetooth, HiperLAN and wireless LAN communication applications. The design is based on IBM SiGe 0.25μm BiCMOS technology which offers good performance and high integration feasibility.

II. INPUT MATCHING

There are several general considerations in LNA designs, including a 50Ω input impedance, the minimum noise figure, maximum gain with sufficient linearity and a low power consumption which is very important for portable systems [8-9]. Recent research shows that the optimum input stage topology is the source inductive

degeneration input stage [9] as described in Fig. 3 (a). Its input impedance can be easily derived,

$$Z_{in} = j\omega L_g + j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{g_{m1}}{C_{gs}} L_s \quad (1)$$
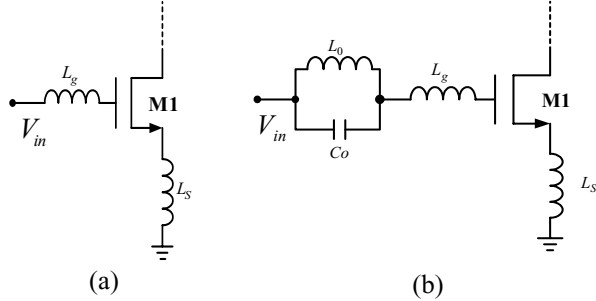

(a)   (b)

Fig. 3. (a) Source inductive degeneration input stage; (b) Input stage for the proposed dual-band LNA in this paper

For input impedance matching purpose, the following equations should be satisfied at the frequency of interest,

$$\left(\frac{g_{m1}}{C_{gs}}\right)L_s = 50 \quad (2)$$

$$j\omega L_g + j\omega L_s + \frac{1}{j\omega C_{gs}} = 0 \quad (3)$$

Solving (3), the resonant/working frequency can be obtained,

$$\omega = 1/\sqrt{(L_g + L_s)C_{gs}} \quad (4)$$

This is the design key of a single-band LNA's input impedance matching. For dual-band/multi-band LNA, the similar methodology can be adopted. There is only one small change - an additional parallel L_0C_0 network is connected to the gate inductor L_g, demonstrated in Fig. 3 (b). In terms of its small signal equivalent circuit, the dual-band LNA's input impedance can be expressed as

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_{m1}}{C_{gs}} L_s + \frac{j\omega L_0}{1-\omega^2 L_0 C_0} \quad (5)$$

To obtain a 50Ω input impedance, the real part and the imaginary part at both resonant frequencies should satisfy:

● Real part:

$$\left(\frac{g_{m1}}{C_{gs}}\right)L_s = 50 \quad (6)$$

● Imaginary part:

$$j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{j\omega L_0}{1-\omega^2 L_0 C_0} = 0 \quad (7)$$

It is obvious that (7) has two solutions at ω_{01} and ω_{02}. Tuning the circuit to resonate at two interested frequency bands such as 2.4GHz and 5.8GHz, giving an L_s value to satisfy (6), a good input matching for a concurrent dual-band LNA for the Bluetooth and WLAN utilizations can be easily realized. The quality of the input matching may greatly influence the overall performance of the designed LNA.
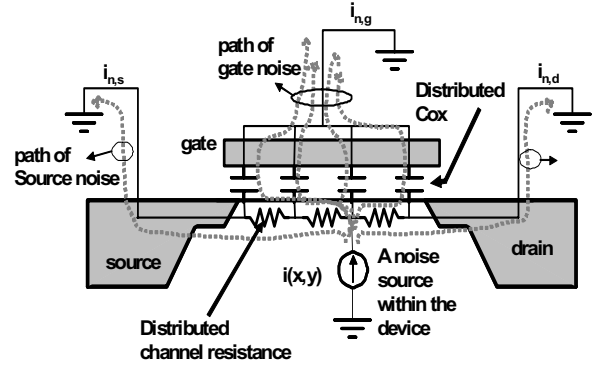

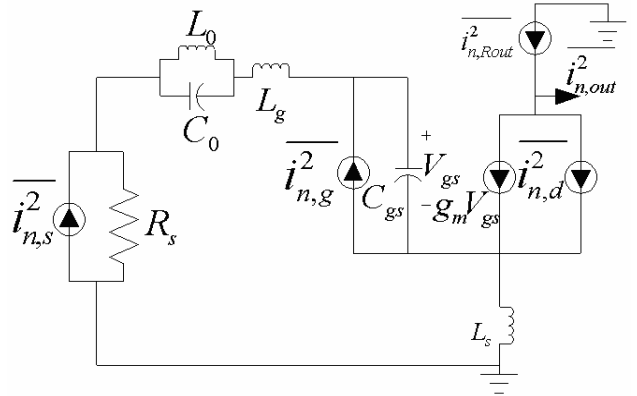Fig. 4. Description of the noise sources in a MOS transistor [10]

Fig. 5. Equivalent circuit with noise sources in the dual-band LNA

III. NOISE OPTIMIZATION

A. Noise Sources

In a MOS device, the prominent noise sources are drain channel noise $\overline{i^2}_{n,d}$, gate induced noise $\overline{i^2}_{n,g}$, distributed gate resistance thermal noise, substrate thermal noise and $\overline{i^2}_{n,corr}$, which is due to the correlation between $\overline{i^2}_{n,g}$ and $\overline{i^2}_{n,d}$. Fig. 4 gives a visual illustration and Fig. 5 depicts an equivalent circuit with noise sources of the proposed dual-band LNA. The noise sources are expressed as follows:

$$\overline{i^2}_{n,R_s} = 4kT \frac{1}{R_s}\Delta f \quad (8)$$

$$\overline{i^2}_{n,R_{out}} = 4kT \frac{1}{R_{out}}\Delta f \quad (9)$$

$$\overline{i^2}_{n,g} = 4kT \delta g_g \Delta f \quad (10)$$

$$\overline{i^2}_{n,d} = 4kT \gamma g_{d0}\Delta f \quad (11)$$

The definitions of the parameters γ, δ, g_{d0} and g_g can be found in [8, 9 and 11].

B. Output Noise and Noise Optimization

Through circuit analysis, the transfer functions of the above noise sources to the output noise current (see Fig.5)

at resonance can be obtained:

$$i_{n,o,R_s} = \frac{g_m}{j2\omega_o C_{gs}} i_{n,R_s} \qquad (12)$$

$$i_{n,o,d} = \frac{1}{2} i_{n,d} \qquad (13)$$

$$\overline{i^2_{n,o,R_{out}}} = \overline{i^2_{n,R_{out}}} \qquad (14)$$

$$i_{n,o,g} = \frac{g_m}{j\omega_o C_{gs}} \frac{j\omega_o C_{gs} R_s - 1}{j2R_s\omega_o C_{gs}} i_{n,g} \qquad (15)$$

$$\overline{i^2_{n,o,corr}} = \frac{g_m |c|}{2\omega_o C_{gs}} \cdot \sqrt{\overline{i^2_{n,g}} \cdot \overline{i^2_{n,d}}} \qquad (16)$$

Then the noise factor F can be obtained,

$$F = \frac{\overline{i^2_{n,o,R_s}} + \overline{i^2_{n,o,g}} + \overline{i^2_{n,o,d}} + \overline{i^2_{n,o,corr}} + \overline{i^2_{n,o,R_{out}}}}{\overline{i^2_{n,o,R_s}}} \qquad (17)$$

$$\approx 1 + \frac{\delta\alpha}{5g_m R_s} + (\frac{\delta\alpha g_m}{5R_s} + \frac{\gamma g_m}{\alpha R_s} + \frac{2|c|g_m}{R_s}\sqrt{\frac{\gamma\delta}{5}})(\frac{\omega_0}{\omega_T})^2 R_s^2$$

Substitute the operating frequencies ω_{01} and ω_{02} into (17), the corresponding noise factors can be easily got. One also can do noise optimization according to (17). After a complicated analysis and derivation process, another expressions for F is obtained,

$$F = 1 + aQ^2 W^{3/2} + \frac{a}{4}W^{3/2} + bQ^{-1}W^{1/2} + (\frac{1}{d} + \frac{\gamma}{4\alpha d})Q^{-2}W^{-1/2} \qquad (18)$$

where W is transistor width, Q is the quality factor of the input stage network, parameters a, b, d and α are equation coefficients, they are given by

$$a = \frac{\delta\alpha(\frac{4}{3}\omega_o R_s C_{ox}L)^2}{R_s\sqrt{\frac{2u_{eff}C_{ox}I_{ds}}{A_b L}}} \qquad b = \frac{\sqrt{\frac{\gamma\delta}{4}}|c|(\frac{4}{3}\omega_o R_s C_{ox}L)}{R_s\sqrt{\frac{2u_{eff}C_{ox}I_{ds}}{A_b L}}}$$

$$d = R_s\sqrt{\frac{2u_{eff}C_{ox}I_{ds}}{A_b L}} \qquad \alpha = \frac{g_{m1}}{g_{d0}} \qquad (19)$$

A_b is bulk charge factor. It is often set to one in the simplified model of the MOS transistor, but can be significantly larger. Taking derivative of (18) with
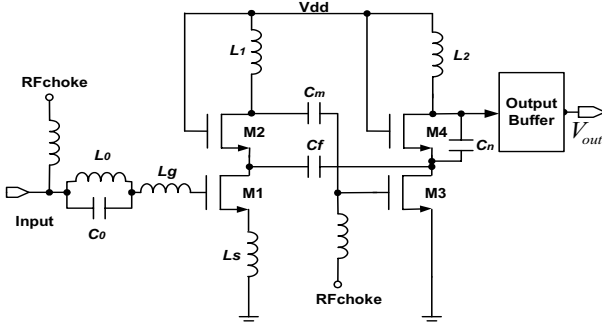
respect to W and equating it to zero, leads to the optimum transistor width W_{opt} corresponding to the minimum NF,

$$W_{opt} = \frac{-\frac{|c|}{2}\sqrt{\frac{\gamma\delta}{4}}Q^{-1} + \frac{1}{2}Q^{-1}\sqrt{\delta\{\frac{\gamma|c|^2}{4} + 3Q^2(4\alpha + \gamma)\}}}{4Q^2\delta\alpha\omega_o R_s C_{ox}L} \qquad (20)$$

However, two W_{opt} values will be achieved here owing to the LNA operating at two different frequencies ω_{01} and ω_{02}. Thus a tradeoff between W_{opt1} and W_{opt2} has to be carried out in terms of the design requirements of different frequency bands.

IV. DUAL-BAND LNA CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

According to the above points, a concurrent dual-band LNA is designed. The simplified schematic diagram is demonstrated in Fig. 6. The LNA is composed of an input matching stage, an intermediate stage and an output buffer stage, which is for output matching purpose. Proper tuning the passive and active devices can make the LNA work at several bands at the same time, which will be very convenient for modern multi-standard communication applications. In the circuit, cascode structure is introduced. Firstly, it is to reduce the Miller effect. Secondly, the use of a cascode improves the LNA's reverse isolation.

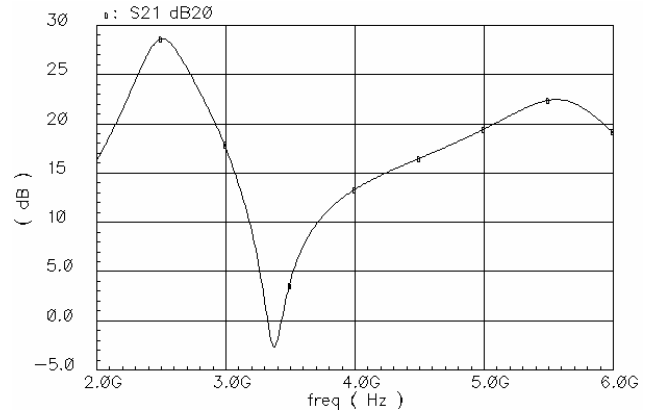The designed dual-band LNA is based on IBM 0.25μm SiGe BiCMOS technology, using only CMOS devices.
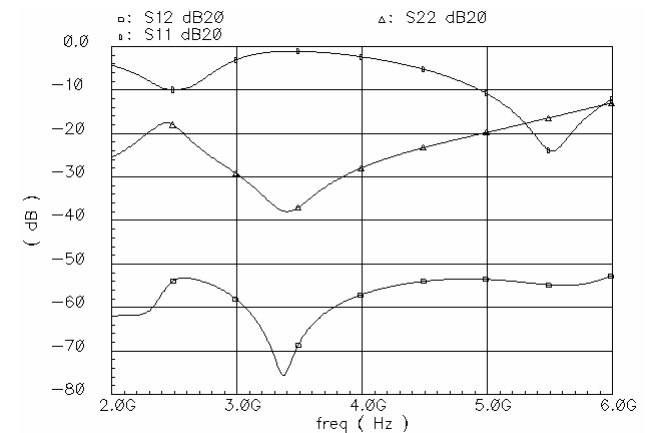

Fig. 7. Simulation result of the power gain

Fig. 6. Schematic diagram of the dual-band LNA

Fig. 8. Simulation results of S_{11}, S_{12} and S_{22}

As known, GaAs offers the best performance. However it is costly and its back gating and side effect limit the degree of integration. Silicon, on the other hand, is
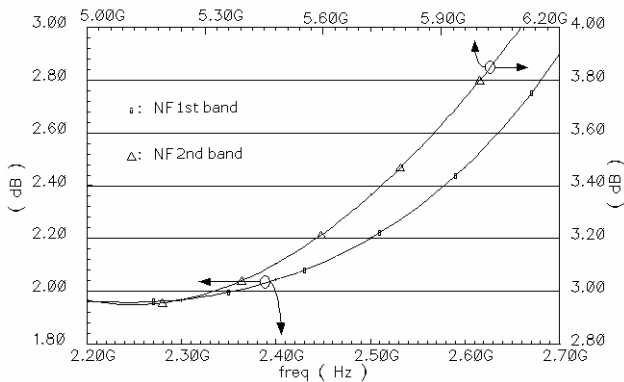

Fig. 9. Simulation result of *NF* of the proposed dual-band LNA

abundant in nature and allows a high degree of integration. Unfortunately, silicon suffers from a lossy substrate, which restricts the quality of the on-chip passive components. While SiGe BiCMOS technology offers a comfort level (lower cost, higher integration) for silicon designers. It is especially well suited to portable wireless applications where its characteristics offer significant advantages [12].

The proposed dual-band LNA is simulated with Cadence Spectre RF. Fig. 7 – Fig. 9 illustrate the simulation results of S-parameters. The plots indicate that the LNA has a gain of about 27 dB at the first band and a gain about 20dB at the second band. The LNA's detailed performance can be found at Table I.

TABLE I
DETAILED PERFORMANCE OF THE DUAL-BAND LNA

	1st band	2nd band
Vdd (V)	1.5	
Pd (mW)	21	
Operating Band (GHz)	2.35 - 2.6	5.0 - 6.0
Standards Covered	Bluetooth, IEEE802.11b/g	HiperLAN, IEEE 802.11a
Gain (dB)	26 - 28.6	19 - 22
S_{11} (dB)	-10 - -9	-24 - -11
S_{22} (dB)	-20 - -17.5	-19.8 - -13
S_{12} (dB)	-60 - -20	
NF (dB)	2 - 2.2	2.95 - 3.8
P_{1dB}(dBm)	About -10	

VI. CONCLUSION

A concurrent dual-band low noise amplifier for the Bluetooth, HiperLAN and Wireless LAN applications is presented in this paper. The LNA is implemented entirely on a single-chip and is possible to be integrated with other building blocks based on SiGe 0.25μm BiCMOS technology.

It has lower cost as well as better integration feasibility comparing with GaAs devices, while better performance comparing with silicon devices.
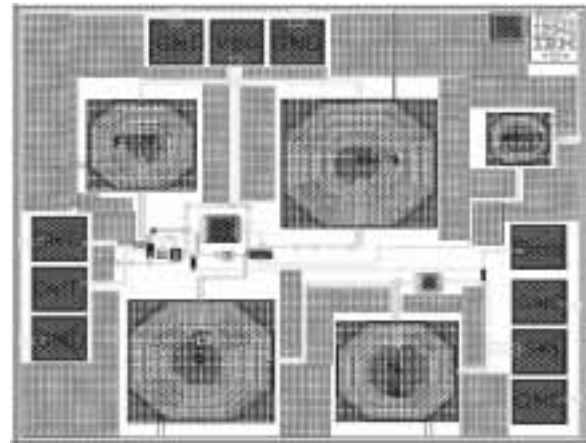

Fig. 10. Layout of the proposed dual-band LNA

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