Dual Band Monolithic AGC Amplifier for Space Applications based on a commercial 0.2 µm PHEMT Technology

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Abstract — This paper reports the design and measurement of a dual band monolithic AGC amplifier to be used in transmit/receive modules for Telemetry, Tracking and Control (TTC) of satellite systems. The amplifier is also included in a multifunction Monolithic Microwave Integrated Circuit, MMIC, containing frequency converters. The block diagram of this chip is shown in figure 1. The goal of the work is to reduce the number, size, and consequently, the cost of the circuitry actually in use, whilst maintaining performance, through the use of mature GaAs PHEMT technology. Issues such as circuit topologies, dc power consumption, circuit area minimization and optimization are all important factors that are addressed during the design.

I. INTRODUCTION

Reducing physical dimensions, whilst maintaining optimum performance, is a general rule for new electronic equipment. This is essential for satellites and space modules that need complex transmit/receive circuits with very demanding requirements.

The design of electronic equipment has undergone a dramatic change due to the use of MMIC. It has permitted a reduction in mass and cost by a factor of two from the previously employed discrete hybrid family [1], whilst not maintaining but increasing the reliability of equipment. Transceiver subsystems using MMIC chips have recently been developed for communication applications. However the multiple MMIC chip assembly solution results in a greater manufacturing and tuning time, which results in higher costs. GaAs PHEMT Technology offers a solution to this problem through multifunctional chips with higher yields and a higher level of integration at the chip level, so reducing the number of chips and resulting in a lower test and module assembly cost. Multifunctional can be defined as a circuit that includes several building blocks, integrated in such a way to minimise the size of GaAs surface and interface, that contribute to the realization of one or more complex functions [2].

The technology [3], process and foundry used have been chosen using two criteria. The first is that good performance is ensured, while the second is in relation to the very strict spatial requirements [4],[5]. The OMMIC foundry has one of the few European processes with which meets these requirements for realising our AGC design.

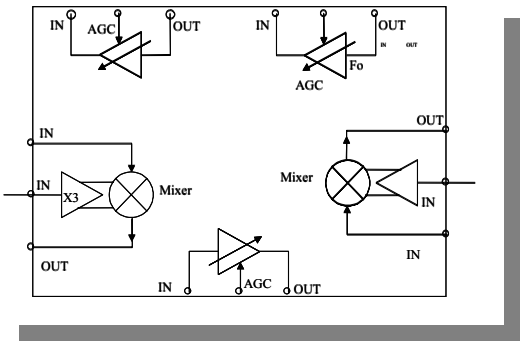


Fig. 1. Block diagram of the MMIC.

The designed AGC has a gain control range of 30 dB. Most of its features are independent of the gain value: the P1dB is almost constant within the gain control range; the same happens with the OIP3. One of the most critical features of this design has been that of the group delay degradation as well as the Output Power at 1 dB gain compression degradation. The measured characteristics of the first prototype are very similar to that of simulation.

II. MMIC DESIGN

For the complete circuit design the HPMDS version 7.2 and ADS version 1.7 from Agilent Technologies were used. The design kit provided by the foundry included the full set of model parameters for linear and non linear simulations, as well as parameters for noise simulations. Cadence tools were later used for the final design rule checking (DRC).

From this a Three Stage Variable Gain Amplifier has been designed [6], [7]. Figure 2 shows its configuration. The first stage provides the input match required by the technical specifications, i.e. better than 15 dB and 10 dB of voltage gain. The second one provides the majority of the gain, with a typical common source configuration. The third one, a source follower configuration, provides the rest of the gain and the power characteristics, such as P1dB and OIP3. The amplifier shows a maximum gain of 42 dB with a 66 % bandwidth at 9 MHz and a gain control range of 30 dB. A negligible OIP3 degradation is achieved with this design topology.

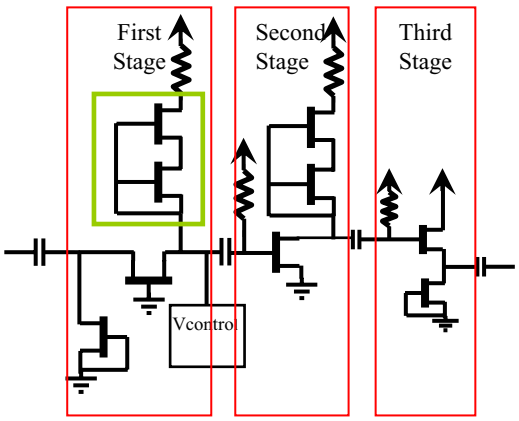


Fig. 2. Architecture of the AGC.

One of the main aims has been to reduce the dc power consumption because of the problem of heat dissipation in space applications. For that reason the size and the polarization of every transistor has been optimised to obtain the best power behaviour, without an unnecessary increase of dc power consumption.

The group delay degradation has been one of the most important and critical design features, the maximum degradation allowed being 1 ns. At 178 MHz this parameter is not as critical as it is at 9 MHz, where the amplifier has a bandwidth of 66 %. The main problems appeared at the decoupling stages and in the design of the internal RF chokes. With regard to the decoupling stages, there are technology limitations on the availability of the electrical component values and dimensions. It was desirable that RF chokes be internal inductors, however, in this case the component values were not technologically possible either. Therefore, instead of the inductors we have used a double active charge, with transistors that can be seen inside the green square of Figure 2. Finally, the group delay degradation obtained is 0.9 ns.

The amplifier has similar characteristics at 178 MHz. In this case the maximum gain is 40 dB with a bandwidth of 25 %. The gain control range is 30 dB, the OIP3 is 17 dBm and its degradation is negligible too. The group delay degradation is less than 50 ps, which is much better than that of the 9 MHz band.

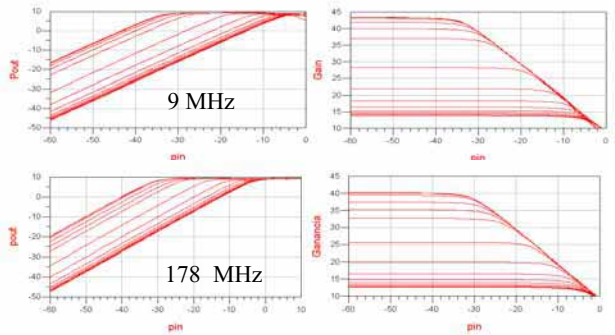


Fig. 3. Output power and gain of the AGC chip as a function of input power for fixed frequency, parameterized by Vcontrol, with Vcc = 3.5 V.

A simulation of the output power and gain for the AGC chip at the central frequency of each of the 9 MHz and 178 MHz bands, as parameterized by control voltage, Vcontrol, is seen in Figure 3.

III. MEASUREMENTS

The layout chip, shown in Figure 4, contains amplifiers and frequency converters that will be used for signal amplification and up/down conversion. The area of the MMIC is 5mmx5mm.

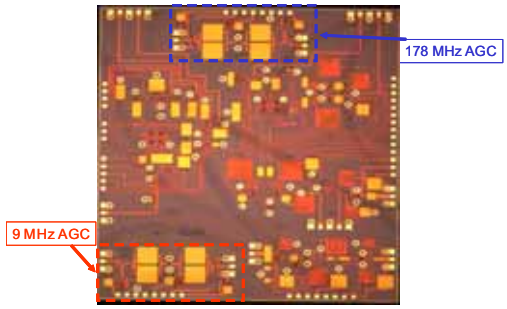
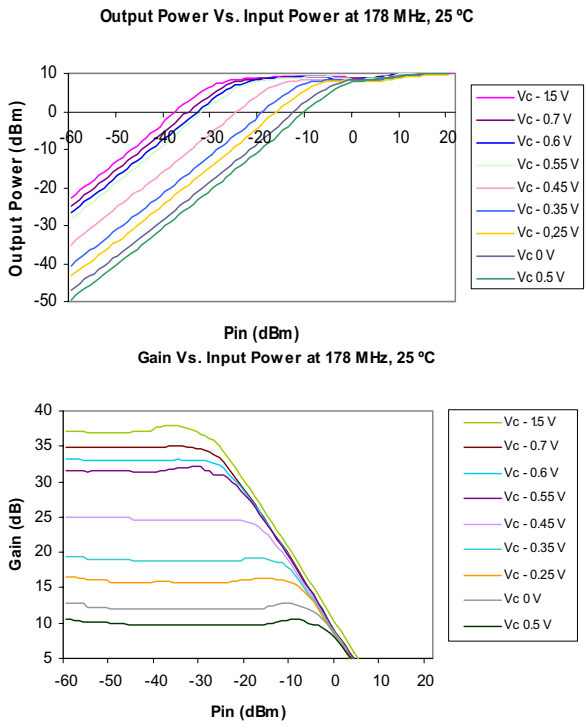


Fig. 4. Layout of the measured MMIC.

A. Ambient Temperature, 25 ºC

Three kinds of measurements have been realized: small signal, obtaining the S Parameters, input and output match and small signal gain; large signal, obtaining gain, Output Power at 1 dB gain compression and Output Intercept Point; and noise, measuring the noise figure. The Figure 5 shows the output power and gain as a function of the input power, and the gain as a function of the control voltage, Vcontrol, for a fixed frequency of 178 MHz.



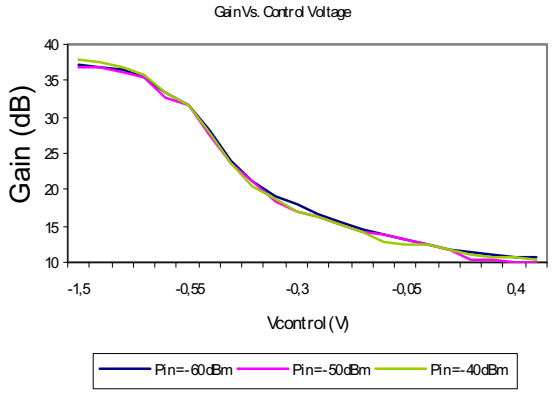


Fig. 5. Output power and Gain as a function of the Input Power at 178 MHz parameterized by Vcontrol. Gain as a function of Vcontrol.

In the bellow table, Table 1, the values from simulation and measurement can be seen as comparable.

Parameter	Simulation Characteristic	Measurements Characteristic
Power Supply	3.5 V	3.5 V
Circuit Current	24 mA	28.5 mA
Centre Frequency	9 – 178 MHz	9 – 178 MHz
Input Return Loss	17 dB	15 dB
Maximum Power Gain	42 - 40 dB	41 – 37 dB
Gain Flatness	< 0.5 dB	< 0.5 dB
AGC Dynamic Range	30 dB	30 dB
Output Intercept Point (OIP3)	17 dBm	17 dBm
OIP3 Degradation	0 dB	0.5 dB
Output Power at 1 dB gain compression	7 dBm	7 dBm
Saturated Output Power	10 dBm	10 dBm
Noise Figure	7 dB	10 dB
Group Delay Non Linearity	0.5 ns	< 1 ns

Table. 1. Simulated and measured performance of the AGC.

B. Temperature Range

Another requirement for this circuit is that the amplifier should work correctly across a wide range of temperatures: from – 30 to 65 ºC, and therefore the measurements made at 25 ºC were repeated at these limits. At 9 MHz and 178 MHz bands the behaviour of power measurements are similar: when the temperature decreases the maximum gain and the gain control range decrease too; whereas, when the temperature increases, these parameters also increase.

Figure 6 shows the output power and gain as a function of the input power for a fixed frequency of 178 MHz at – 30 and 65 ºC, respectively. In both cases the maximum and the minimum gain have changed from that at 25 ºC. At 65 ºC there is only a slight difference but at – 30 ºC the maximum gain and the gain control range have notable decreased: to 27.8 dB and 27 dB, respectively. The OIP3 and the remaining features follow a similar temperature trend.

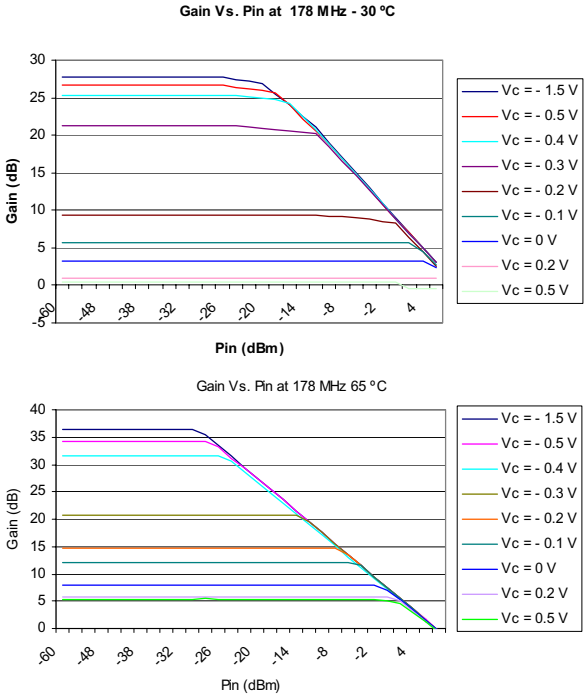


Fig. 6. Output power and Gain as a function of the Input Power at 178 MHz parameterized by Vcontrol, at – 30 and 65 ºC.

IV. SECOND PROTOTYPE

Another version has been designed and simulated in order to avoid some critical aspects of that of the first. One of these aspects relates to the high sensitivity of the amplifier to some of the polarization voltages. In the new version, we have substituted them for other voltages to which the circuit is less sensitive and is, therefore more robust. Second and third stages are DC coupled, minimizing the contribution of capacitors to group delay degradation and decreasing the chip size. In the second stage depletion and enhancement transistors have been combined, such as to avoid an excessive increase of circuit current, as well as to keep and also improve some features. The size of the new chip is 1mmx2mm.

In the bellow table, Table 2, the values from simulation can be seen. The main differences between the first and second prototype results are the increases of the P1dB, OIP3 and circuit current in the second.

Parameter	Simulation Characteristic
Power Supply	3.5 V
Circuit Current	28 mA
Centre Frequency	9 – 178 MHz
Input Return Loss	19 dB
Maximum Power Gain	40 – 37 dB
Gain Flatness	< 0.5 dB
AGC Dynamic Range	31 dB
OIP3	19 dBm
OIP3 Degradation	1 dB
P1dB	9 dBm
Sat. Output Power	10 dBm
Noise Figure	7 dB
Group Delay Deg.	0.95 ns

Table. 2. Simulated performance of the AGC.

Actually, this circuit is being built, and after that it will be measured.

V. CONCLUSION

This paper has described the design and measurement of a dual band monolithic variable gain amplifier to be used in space applications. The gain control range of 30 dB, the P1dB of 7 dBm, the P1dB degradation less than 1 dB and the group delay degradation less than 1 ns are the main features obtained. It has been presented along with its simulated and measured values, including its temperature behaviour.

ACKNOWLEDGEMENT

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