Ka-band Coplanar Low-Noise Amplifier Design with Power PHEMTs

Sabine Long[1], Laurent Escotte[1], Jacques Graffeuil[1], Philippe Fellon[2] and Daniel Roques[3]

[1] LAAS CNRS et Université Paul Sabatier, 7 Av. du Colonel Roche, 31077 Toulouse cedex 4, France
e-mail : escotte@laas.fr, phone : 33 (0)5 61 33 64 56, fax : 33 (0) 5 61 33 69 69
[2] United Monolithic Semiconductors, 91041 Orsay cedex, France
[3] Alcatel Space, 26 Av. J.F. Champollion, 31037 Toulouse cedex, France

***Abstract* — The design of a coplanar low-noise amplifier (LNA) is presented in this paper. Pseudomorphic high electron mobility transistors (PHEMTs), optimized for power applications, are used in order to evaluate the potentiality of this technology for mixed-mode applications. The three stages amplifier noise figure is lower than 2.6 dB on the 27 - 31 GHz frequency band with a 20 dB power gain.**

I. Introduction

A cost reduction of circuit design and production for mixed-mode (low noise / power) applications could be achieved using only one kind of component. The number of component modeling steps is then reduced and the low-noise and power circuits are fabricated at the same time. This cost saving can further be improved by using a flip-chip assembly which achieves simultaneously the mechanical and electrical link between the chip and its mounting substrate. Moreover, flip-chip report is automatizable and compact [1] and thermal bumps implemented on the source pads of the transistors reduce the thermal resistance of the devices [2]. However, it makes necessary the use of a coplanar technology in order to decrease the carrier substrate detrimental influence on the circuit behavior [3]. Coplanar LNA have been yet realized in V and W-band [4]-[5], but this technology is not currently used in Ka-band.

We present in this paper the design of a Ka-band coplanar low-noise amplifier (LNA). This circuit is based on pseudomorphic high electron mobility transistors (PHEMT) optimized for power applications and fits the prerequisites of flip-chip assembly. The transistor noise characteristics are described in the second section and compared with those of a more classical low-noise PHEMT. The third section is dedicated to the circuit design and the simulation results are given in section four. Experimental results are reported in the last section.

II. Device Characteristics

The 0.25 µm gate length GaAs-power transistors are AlGaAs/InGaAs PHEMTs of the United Monolithic Semiconductors (UMS) foundry and feature a double-heterojunction (DH). The second heterojunction, located under the channel, improves the power performances of the transistor. It allows a higher number of free electrons to travel along the channel, and then, provides a higher maximal drain current, I_{dmax}. The device also features a double-recessed gate which increases the breakdown voltage [6].

The high frequency noise of these components is compared to those of conventional low-noise single-heterojunction PHEMTs (SH-PHEMT) elsewhere [6]. The noise parameters of these two kinds of transistors are very close, as shown in Fig. 1, even if the technologies are optimized for different applications. The minimum noise figure F_{min} features a 1.6 dB minimum at 30 GHz for a drain current equal to 75 mA/mm.

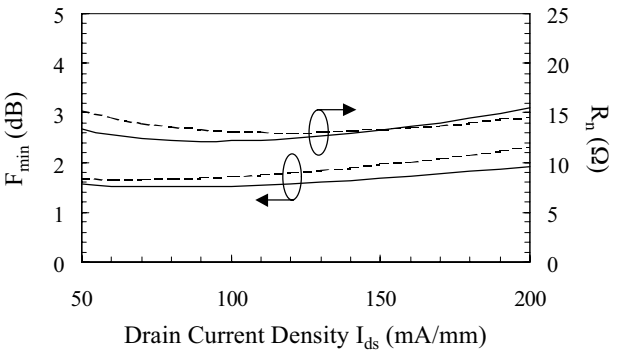

Fig. 1. Minimum noise figure F_{min} and equivalent noise resistance R_n variations against drain current density at 30 GHz and V_{ds} = 2V. - - -: DH-PHEMT; —: SH-PHEMT.

The small-signal and noise model of the power transistors are extracted from scattering and noise parameter measurements carried out up to 40 GHz. The noise parameters are measured using a Ka-band source-pull test bench developed in our laboratory [7]. This model is scalable in terms of gate geometry (width and number of gate fingers) and drain current I_{ds}.

III. Circuit Design

The objective was to design a 20 dB gain MMIC amplifier that covers the 27-31 GHz frequency band. A three-stage circuit topology was chosen to achieve the targeted specifications. The gate geometry and bias conditions of the two first stages are selected in order to

minimize the noise figure. To this end, each of the four noise parameters and the associated gain are considered. We select a component having a minimum noise figure together with an equivalent noise resistance R_n as low as possible. This last feature reduces the noise figure increase in case of a minor noise mismatching.

The variations of F_{min} and R_n against gate geometry are reported in Fig. 2 at 30 GHz and I_{ds} = 100 mA/mm.

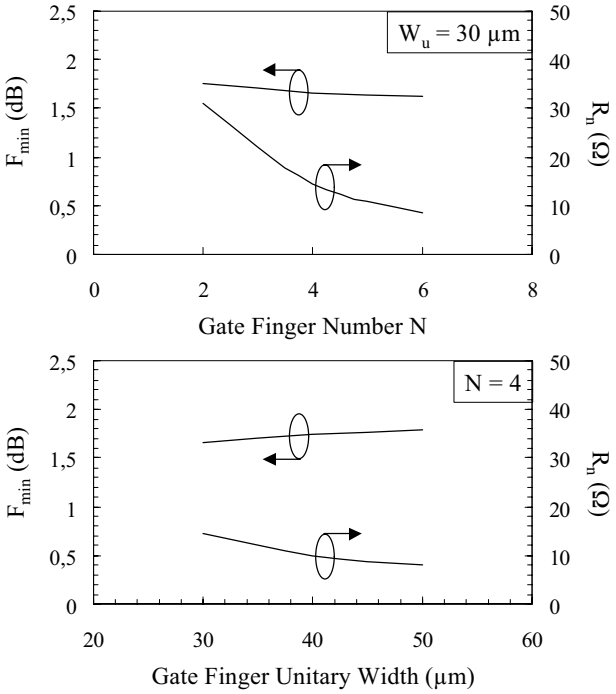

Fig. 2. Minimum noise figure F_{min} and equivalent noise resistance R_n variations against gate geometry at 30 GHz and I_{ds} = 100 mA/mm.

An increase of the gate number N considerably decreases R_n and, to a lesser extent, F_{min}. A decrease of the gate finger width W_u decreases F_{min} and slightly increases R_n. The associated gain is also higher for the smallest devices. Finally, a component featuring a high N (= 6) and small W_u (= 30 µm) is selected.

The choice of drain current value results from a tradeoff between F_{min} and R_n. As shown in Fig. 1, the minimum of F_{min} is obtained for a drain current equal to 75 mA/mm and the R_n minimum for 120 mA/mm. A drain current equal to 85 mA/mm is then chosen for each transistor leading to a total drain current equal to 57 mA for the LNA.

Finally, the transistor dimensions of the last stage are taken higher than those of the two first stages (6×50 µm instead of 6×30 µm) in order to improve the linearity of the amplifier. The voltage bias conditions of the three stages are then identical (V_d = 2.2 V and V_g = - 0.3 V).

The circuit design was performed using ADS (Agilent®) and COPLAN (IMST) softwares. The passive elements are simulated with COPLAN using a physical description (height and width of the different layers).

The layout and the schematic diagram of the Ka-band MMIC LNA are shown in Fig. 3.

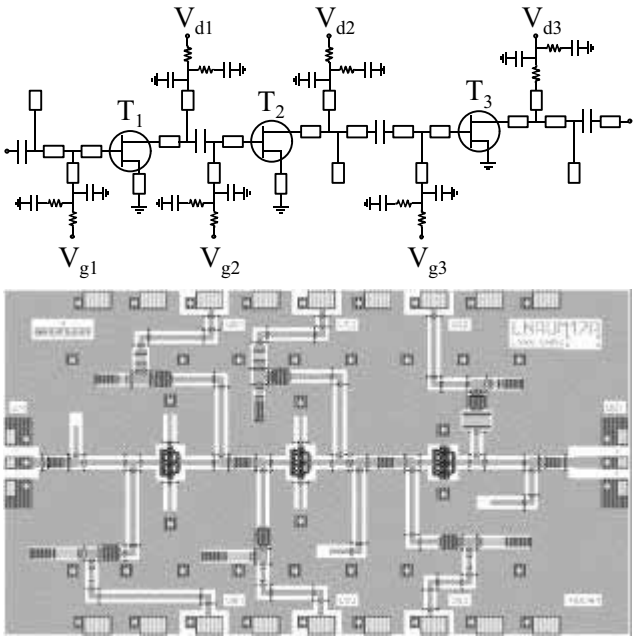

Fig. 3. Topology and layout of the coplanar low-noise amplifier (3.5 × 2 mm²).

Inductive short-circuited lines connected to the source electrodes of the two first transistors are used to ensure stability and to bring together the optimum noise reflection coefficient Γ_{opt} and the conjugate of the input reflection coefficient (S_{11}*). The third stage is stabilized using a shunt TaN resistance located on the drain.

Matching networks are based on coplanar transmission lines. Air-bridges are used at each discontinuity in order to suppress any undesired slotline mode on the coplanar waveguide (CPW). RC networks are added in the bias circuits in order to avoid low-frequency oscillations. Inter-stage MIM capacitors are used for DC-blocking.

Cylindrical bumps, with 30 µm diameter and height, are laid out on the circuit to allow the further flip-chip assembly [2]. Microwave and bias probe pads are also added in the layout in order to be able to measure the amplifier before the flip-chip report.

IV. Simulation Results

Simulation results are reported in Fig. 4 and Table I. The noise figure F_{50} is 2.6 ± 0.2 dB in the 27-31 GHz frequency range with a 20 dB gain. The input reflection coefficient is lower than - 10 dB and the output one is lower than - 20 dB. The stability has been checked by the way of the Rollett factor K for the entire LNA and for each stage.

The predicted noise figure value is not as good as others previously published data [8]-[9]. Nevertheless it must be recalled that our aim was not to design ultra low-noise amplifiers but only to demonstrate the best noise figure as possible using devices optimized for power applications and featuring a 0.25 µm gate length. Therefore they cannot afford the same noise performance

as 0.15 µm gate length low-noise transistors. It can also be noted that the coplanar technology used for a further flip-chip assembly features higher losses compared to microstrip technology in this frequency range. For these reasons the predicted noise is attractive and demonstrates that power devices can be used for low-noise amplifier design for mixed-mode applications.

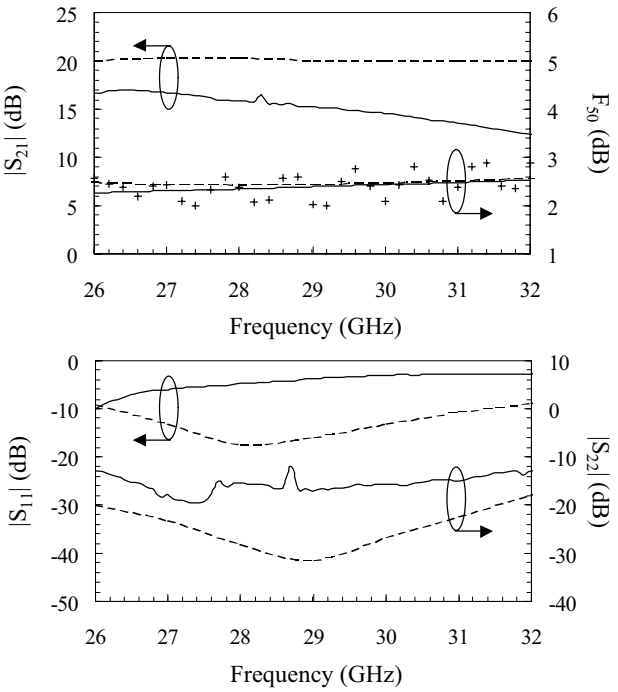

Fig. 4. Simulated and measured characteristics of the LNA at I_d = 57 mA. - - -: simulation; —: measure.

V. Experimental Results

Fig. 4 shows the measured characteristics of the LNA. The measured noise figure is in agreement with the calculated values. All the measurement results at 29 GHz are reported in Table I. The noise figure is equal to 2.4 dB with 15.2 dB gain. It slowly increases with frequency in the 27-31 GHz frequency range from 2.4 dB to 2.6 dB. Unfortunately, the measured S-parameters are strongly different than the simulated values. The gain is lower than expected and further decreases versus frequency from 16.7 dB to 13.6 dB. The measured input reflection coefficient is also higher than the simulated one. Additional measurements below 26 GHz show also a shift in the characteristics (S_{21} and S_{11}) toward lower frequencies.

These unexpected data are related to transistors electrical characteristics that were somewhat different from those found in the foundry design book. This has been verified by measuring a single transistor. The small-signal models of the transistors have then been modified in the simulation files and a retro-simulation was performed. The results are reported in Fig. 5.

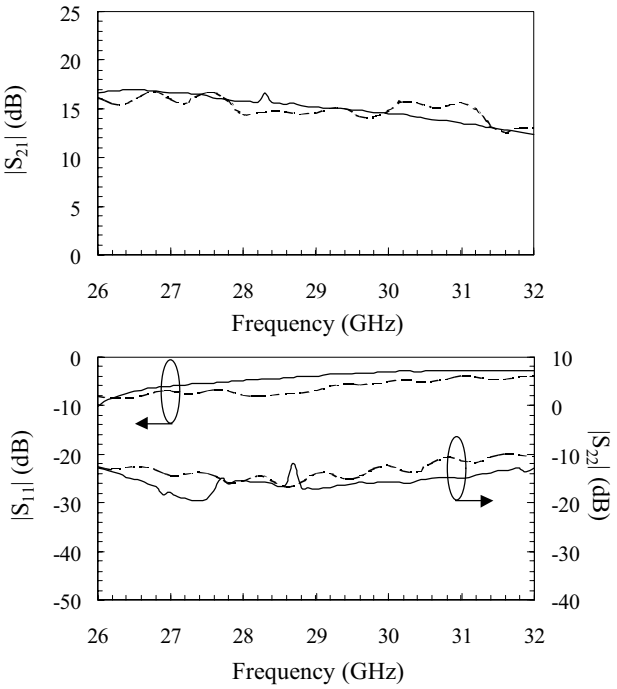

Fig. 5. Retro-simulated with updated transistors data and measured characteristics of the LNA at I_d = 57 mA.
- - -: retro-simulation; —: measurements.

A good agreement is now observed between the retro-simulated values and the experimental results which validate the design technique. The passive elements

Parameter	Simulation		Measurement
	27-31 GHz	at 29 GHz	at 29 GHz
Linear gain	20 dB	20.2 dB	15.2 dB
Gain flatness	0.3 dB		
$\|S_{11}\|$	< - 10 dB	-16 dB	-3.9 dB
$\|S_{22}\|$	< - 20 dB	-31.3 dB	-17.2 dB
Stability	Unconditional	Unconditional	Unconditional
Noise Figure	< 2.6 dB	2.45 dB	2.4 dB
Consumption	125 mW	125 mW	125 mW
Output P_{1dB}	11 dBm	11 dBm	11 dBm

TABLE I
Simulation and Experimental Results

remain unchanged compared to the initial simulations.

VI. Conclusion

A coplanar flip-chip compatible Ka-band low-noise MMIC amplifier design is reported in this paper. A 2.4 dB noise figure with a 15.2 dB gain is obtained at 29 GHz although 0.25 µm gate length power devices were used. The design of this LNA allows a flip-chip assembly which is well suited for applications in the millimeter-wave range. We conclude that DH-PHEMT devices featuring a double-recessed gate and optimized for power applications can be also used for low-noise applications and show a noise behavior similar to the one of conventional PHEMT. It turns out that using a mixed mode single chip for both low-noise and power amplification in modern transceivers is made possible.

Acknowledgement

The authors wish to acknowledge the RNRT (Réseau National de Recherche en Télécommunication) which funded the "OPTIMAL" project (Optimisation en Puissance de Technologies Intégrées Millimétriques pour Amplification Linéaire) that allowed the achievement of this work.

References

[1] C. E. Presley, "FCA: a critical advantage for designers", *Advanced Packaging*, pp. 38-42, Apr. 1999.

[2] E. Rogeaux, J.P. Fraysse, C. Schaffauser, S. George, D. Pons, P. Fellon, D. Geiger, D. Théron, N. Haese, S. Verdeyme, R. Quéré, D. Baillargeat, E. Ngoya, S. Long, L. Escotte, "Ka band power pHEMT technology for space power flip-chip assembly", *IEEE MTT's Digest*, pp. 1895-1898, 2001.

[3] R. Sturdivant, "Reducing the effects of the mounting substrate on the performance of GaAs MMIC flip chips", *IEEE MTT's Digest*, pp. 1591-1594, 1995.

[4] V. Hoel, S. Boret, B. Grimbert, G. Apercé, S. Bollaert, H. Happy, X. Wallart, A. Cappy, "94GHz low noise amplifier on InP in coplanar technology", *Microwave Engineering Europe*, pp. 51-54, Nov. 1999.

[5] A. Fujihara, E. Mizuki, H. Miyamoto, Y. Makino, K. Yamanoguchi, N. Samoto, "High performance 60-GHz coplanar MMIC LNA using InP heterojunction FETs with AlAs/InAs superlattice layer", *IEEE MTT's Digest*, pp. 21-24, 2000.

[6] S. Long, L. Escotte, J. Graffeuil, P. Fellon, D. Geiger, D. Pons, "High-frequency noise in pseudomorphic double-heterojunction high electron mobility transistors", *Fluctuation and Noise Lett.*, vol. 2, n°1, pp. 13-19, Mar. 2002.

[7] S. Long, L. Escotte, J. Graffeuil, F. Brasseau, J.L. Cazaux, "On-wafer noise caracterization of low-noise amplifiers in the Ka-band", *IEEE transaction on Instrumentation. and Measurement.*, to be published in Oct. 2003.

[8] Y. Kwon, D. S. Deakin, E. A. Sovero, J. A. Higgins, "High-performance Ka-band monolithic low-noise amplifiers using 0.2-µm dry-recessed GaAs PHEMT's", *IEEE Microwave and Guided Wave Lett.*, vol. 6, n°7, pp. 253-255, Jul. 1996.

[9] H. Uchida, S. Takatsu, K. Nakahara, T. Katoh, Y. Itoh, R. Imai, M. Yamamoto, N. Kadowaki, "Ka-band multistage MMIC low-noise amplifier using source inductors with different values for each stage", *IEEE Microwave and Guided Wave Lett.*, vol. 9, n°2, pp. 71-72, Feb. 1999.