Characterisation, Modelling and Design of Bond-Wire Interconnects for Chip-Package Co-Design

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ABSTRACT — **This work is a comprehensive experimental investigation of chip to package wirebond interconnects for chip-package co-design. Wirebonds are interconnect bottlenecks in RF design, but are difficult to avoid due to their low cost and manufacturing ease. We have shown measurements on wirebonds in coplanar configuration with different return paths and also the cross coupling. We have also extracted lumped and distributed models and demonstrate the excellent agreement with measurements atleast upto 15GHz. We have proposed multi-wirebonds as a potential solution for better impedance matching. Different types of inductors with Q-factors of upto 100 have also been illustrated. We show influence of encapsulant on wirebonds and finally we also demonstrate a methodology to extract the time-domain response from S-parameters.**

I. INTRODUCTION

Fig.1. illustrates the gain of a 5.2GHz LNA before and after packaging. The reduction in gain of about 2dB is mainly attributed to the impedance mismatch caused by the wirebond. The LNA was designed without any chip-package co-design considerations. The wirebond has a major contribution in the losses of the chip to board interconnect through the package (fig.2).

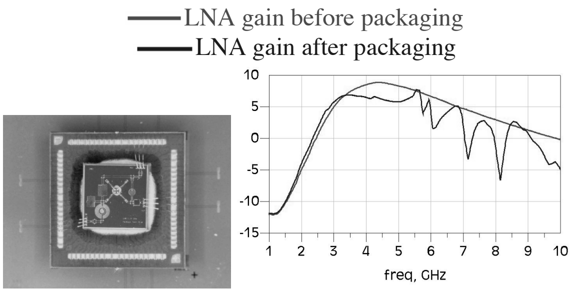

Fig.1. 5.2GHZ LNA gain before and after packaging.

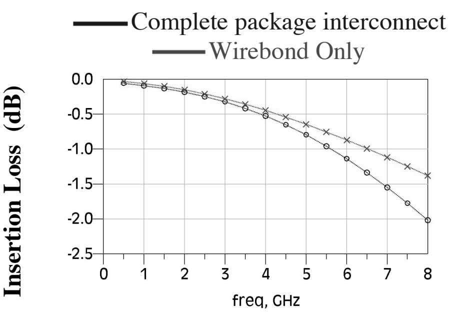

Fig .2. Wirebond contribution total interconnect losses.

Several publications on wirebonds [1], [2] have shown specific methods to get better impedance match, some including passive compensation techniques [3] (which are realtively narrow band solutions). Others use mathematical methods to derive expressions to model these structures [4]. However, our work complements these contributions by encompassing most chip-package co-design issues that can be addressed with wirebonds through experiments as well and model extraction.

An interesting note is that although it is reasonable to assume that flip-chip interconnections give better RF performance over wirebonds, the cost and manufacturing considerations make wirebond applications not easy to replace. This is analogous to developing high-frequency devices with Si and GaAS! Literature is available that show the manufacturing details of wirebonds for RF applications and its comparison with flip-chip.

II. WIREBOND MEASUREMENTS

We have used MCM-D thin film on glass for the carrier substrate and the test chip due to its excellent RF properties and ease of de-embedding (fig.3). Fig.4 illustrates the measurements made on these bonds with different return paths in CPW configuration. We can also see that the corner bond from the chip to the package is quite lossy compared to bond at the centre of the package. The cross coupling of the wirebond to 4 of its neighbours (all sharing the same return path) is illustrated in fig.5. The coupling is less than 20dB to the adjacent interconnect even at 7GHz. The length of the wirebonds in all the cases is about 2mm.

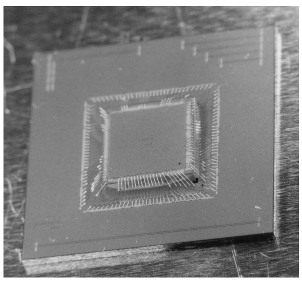

Fig.3. Wirebond test structure on MCM-D thin film on glass.

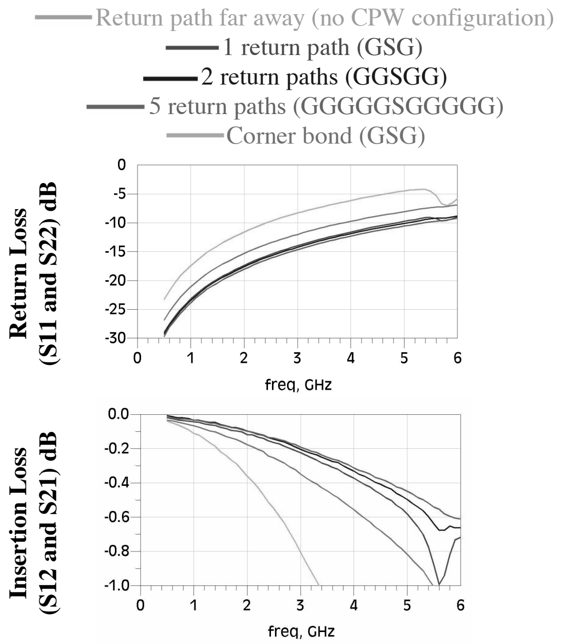

Fig.4. S-parameters of wirebond interconnects with different return paths.

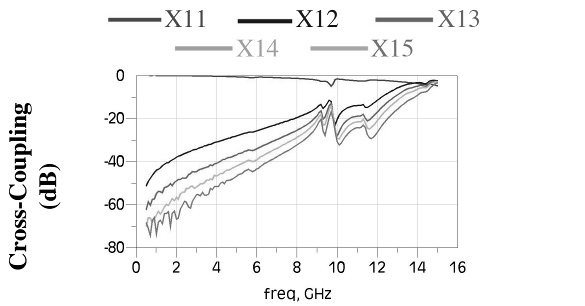

Fig.5. Cross-coupling of wirebond interconnects to the 4 adjacent neighbours.

III. WIREBOND MODELLING

The simplest approach to wirebond modelling is to extract an LC Pi-model [5]. We have also extracted a lumped element model (fig.6) from the wirebond measurements and also converted this to a distributed model (fig.7) using equations 1 to 4. Ref. [6] details the advantages and the flexibility of the distributed model.

$$Z_c = \frac{c_0 L_s}{\ell\sqrt{\varepsilon_{eff}}} \tag{1}$$

$$E = \frac{\omega_c \ell \sqrt{\varepsilon_{eff}}}{c_o} \tag{2}$$

$$C_a = C_1 - \frac{1-\cos\beta\ell}{\omega_c^2 L_s} \tag{3}$$

$$C_b = C_2 - \frac{1-\cos\beta\ell}{\omega_c^2 L_s} \tag{4}$$

where Z_c and E (electrical length $\beta\ell$) are the transmission line parameters, L_s, C_1 and C_2 are the lumped element values and C_a and C_b are the distributed element values.

The models agree very well with measurements (fig.8) with the distributed model showing a marginally better agreement with the measurements.

We have also verified the measurements with Ansoft HFSS simulations (fig.9).

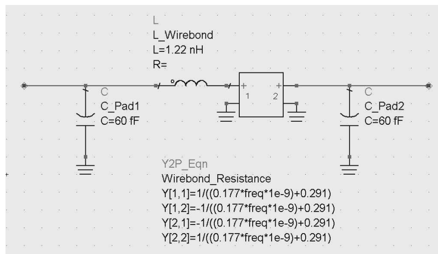

Fig.6. Lumped element model of a wirebond.

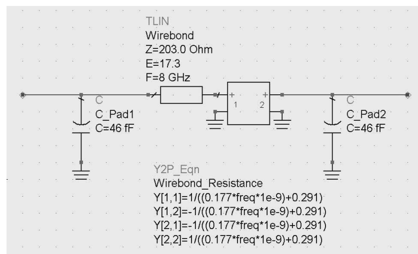

Fig.7. Distributed model of a wirebond.

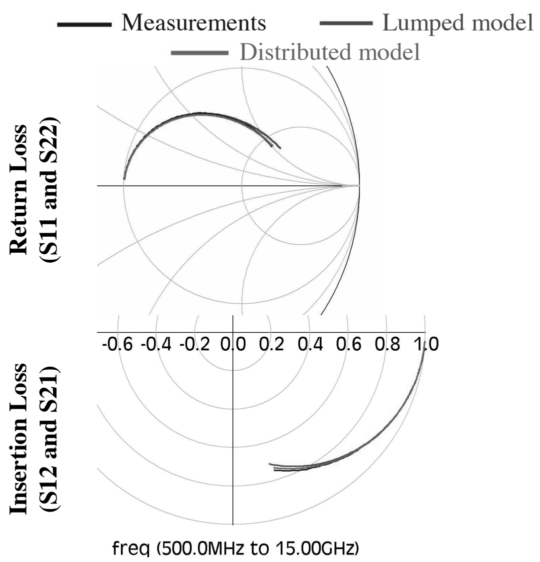

Fig.8. Comparison of models with measurement.

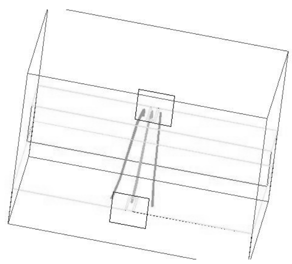
Fig.9. Model of a CPW wirebond for 3D simulations.

IV. MULTI-WIREBONDS FOR BETTER IMPEDANCE MATCHING

The fastest, most cost effective and broadband solution for reducing impedance mismatch is to use multi-wirebonds [7], [8]. While ribbon bonds are very slow and expensive, compensation techniques provide only a narrow band solution at the expense of area. Figs 10 and 11 show multi-wirebond structures with a ground plane underneath and the RF performance. We also show that the absence of the ground plane below the bonds has an influence only when the wirebond spacing is large. Figs. 12 and 13 demonstrate the same but with wirebonds in the ground path also instead of a ground plane. We can see that even 3 return paths still cannot provide the performance of a ground plane.

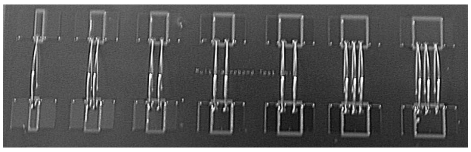

Fig.10. Multi-wirebonds with a ground plane underneath.

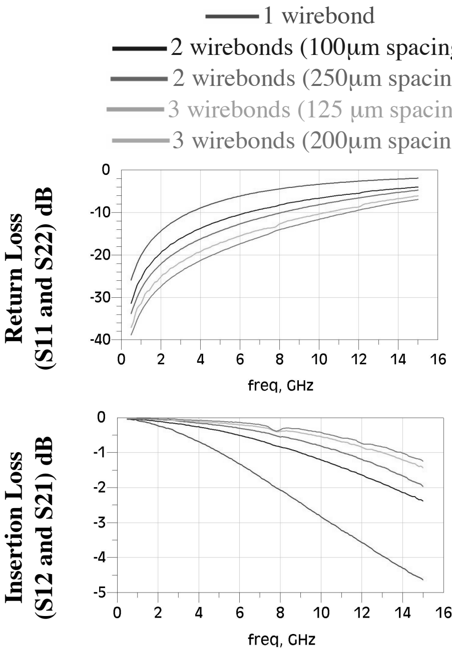

Fig.11. S-parameters of multi-wirebonds.

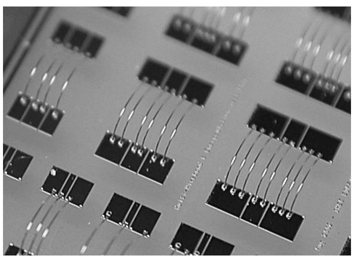

Fig.12. Double bonds with multi-wirebonds for the return path.

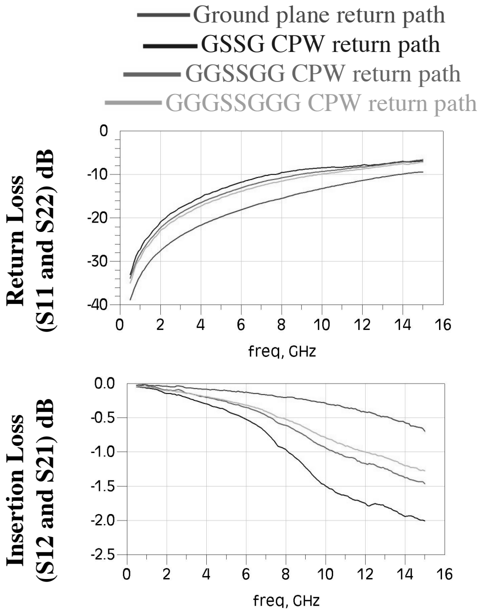

Fig.13. S-parameters of a double-bond with multi-wirebonds in the return path

V. HIGH-Q INDUCTORS USING WIREBONDS

We have built, measured and simulated 3 types of wirebond inductors [9]-[11] namely chip to package loops (fig.14), 3D spirals (Fig.14) and the multi-wirebonds (fig.14). The Qmax obtained with the different types are summarised in fig.15 and in table. 1. The double bond inductors give the highest Q with the smallest pads and the closest spacing between the bonds.

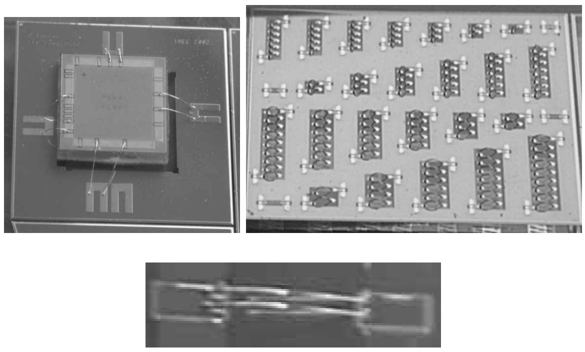

Fig.14.Chip to package loop inductor (top left), 3D spiral inductor (top right) and double bond inductor(bottom).

Table. 1. Performance of the different wirebond inductors

Inductor Type	Qmax	Freq_Qmax	L at Qmax
Chip to Package Loop	29	1.3 GHz	4.42 nH
3-D Spirals	21	3 GHz	4.6 nH
Double Bonds	100	4 GHz	1.36 nH

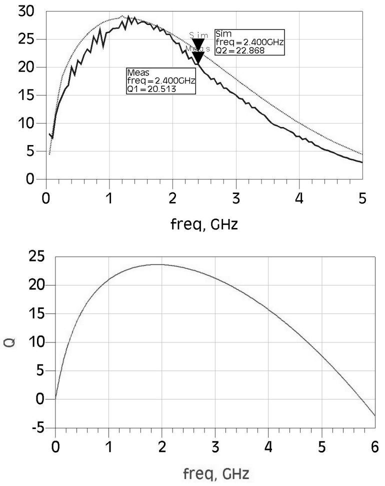

Fig.15. Q-factor plots of chip-package loop inductor (top) and 3D-spiral (bottom).

VI. INFLUENCE OF ENCAPSULANT ON WIREBONDS

We have studied the influence of gloptop on the wirebond [12]. Fig.16 shows the loss of an encapsulated wirebond with ε_r=4 and varying tanδ. The influence of tanδ>0.1 is significant.

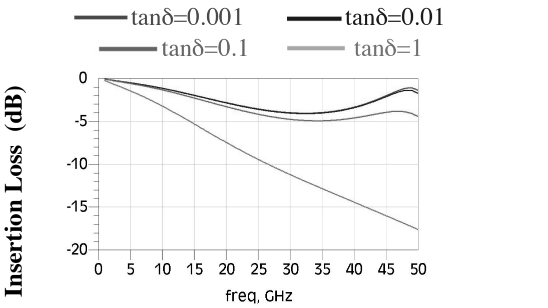

Fig.16. Loss of encapsulated wirebond (ε_r=4).

VII. EXTRACTION OF TIME-DOMAIN PERFORMANCE FROM S-PARAMETERS

With a wealth of S-parameter data available, it is very straightforward to study the time-domain performance of the wirebond interconnects. We have transformed the frequency-domain data to time-domain data. The input signal has a 50ps rise time and a 10Ω impedance, while the load is a 5pFcapacitance (fig. 17). We can see that the wirebond transforms a typical RC interconnect into an RLC interconnect leading to ringing. It is also very interesting to note that the effect of multiple return paths is insignificant for digital signals which is otherwise for RF analogue signals.

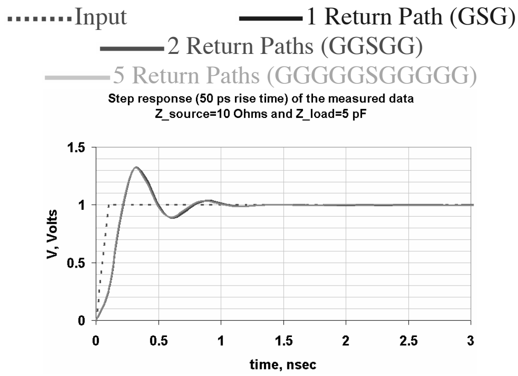

Fig.17. Time-domain performance of wirebonds with multiple return paths.

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