A 5.8 GHz Mixer using SiGe HBT Process

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***Abstract* — DSRC provides high speed radio link between Road Side Equipment and On-Board Equipment within the narrow communication area. In this paper, a 5.8 GHz down-conversion mixer for DSRC communication system is designed and fabricated using 0.8 µm SiGe HBT process technology and RF/LO matching circuits, RF/LO input balun circuits and IF output balun circuit are all integrated on chip. The measured performance is 7.5 dB conversion gain, -2.5 dBm input IP3, 46 dB LO to RF isolation, 56 dB LO to IF isolation, current consumption of 21 mA for 3.0 V supply voltage and the chip size of fabricated mixer is 1.9 mm X 1.3 mm.**

I. INTRODUCTION

ITS (Intelligent Transportation Systems) technology has been developed to solve the traffic problem such as traffic congestion and accidents and reduce the overall congestion cost. The final goal of ITS will be to improve the traffic efficiency and mobile safety without new road construction. DSRC (Dedicated Short Range Communication) provides high speed radio link between Road Side Equipment (RSE) and On-Board Equipment (OBE) within the narrow communication area. DSRC communication system has been developed worldwide and recently applied for Electronic Toll Collection (ETC), but most of all ITS services will be provided by DSRC communication [1].

The SiGe hetero-junction bipolar transistor (HBT) has been considered to be more suitable for RF integrated circuits than the Si bipolar junction transistor (BJT) because its electrical properties, such as current gain, power consumption, small-signal unity-gain frequency, and maximum oscillation frequency are superior to those of the Si BJT [2]. Because of having many advantages for those RF applications, SiGe HBT device has been adopted as a good candidate for manufacturing RF components such as LNAs, Mixers, VCOs, PLLs, RF transceivers.

Down-conversion mixers, which convert radio frequency (RF) signal to intermediate frequency (IF) signal, are very important building blocks within a radio system. Their performance affects the performance requirements of the entire system and the performance requirements of other building blocks.

In this paper, a 5.8 GHz down-conversion mixer including RF/LO matching circuits, RF/LO input balun circuits and IF output balun circuit for DSRC receiver is designed and fabricated on chip, using SiGe HBT process technology of Electronics and Telecommunications Research Institute (ETRI). The measured performance was 7.5 dB conversion power gain, -2.5 dBm input IP3, 46 dB LO to RF isolation, 56 dB LO to IF isolation, current consumption of 21 mA for 3.0 V supply voltage.

II. SIGE HBT DC AND AC CHARACTERISTICS

Electrical performance parameters of SiGe HBT such as cut-off frequency (f_T), maximum oscillation frequency (f_{max}), minimum noise figure (NF_{min}) are critically dependent on not only the base thickness, but also the fabrication process. We used RPCVD system to grow base epitaxial layer, and adopted LOCOS isolation to separate device and device terminals. The maximum values of f_T/f_{max} were 41 GHz/42 GHz at V_{CE} = 2V, I_C = 1.83mA as shown in Fig. 1. In Table 1, the main DC and AC parameters of HBT with emitter area of 0.5 × 6.0 μm^2 are summarized. Passive elements used in this paper were MIM capacitor, parallel-branch spiral inductor, and resistors composed of metal, emitter poly-silicon, and base poly-silicon.

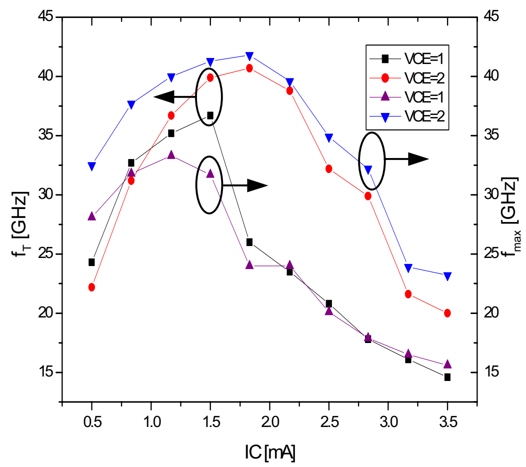

Fig. 1. AC characteristics of SiGe HBT

III. SIGE HBT MIXER DESIGN

The architectures of DSRC RF front-end receiver and down-conversion mixer in this receiver are shown in Fig. 2. The LNA output and LO output signals go RF single input port and LO single input port of mixer, respectively, and single output signal of mixer goes IF input port. The 5.81 GHz single-ended RF input and the 5.495 single-ended LO input are converted to be differential to feed in the double balanced mixer by use of on-chip active balun.

Fig. 3 shows the single-input, balanced-output differential balun, which is used as the RF and LO balun. In this Fig. 3, the single input is applied to the base of transistor Q1, and the output is measured between the two collectors, which are at the same dc potential. The gain of balun is determined by transconductances of Q1, Q2, the degeneration inductors L1, L2, and the output resistors R1, R2. The amount of the LO suppression is determined by the common-mode gain of the balun, and the differential-type balun rejects very well the common-mode gain. The higher the output impedance of the current source, the better the LO suppression [3,4]. The capacitor C1 separates DC bias from ground.

Table 1. SiGe HBT DC & AC Characteristics

Emitter area [μm^2]	0.5 × 6.0
DC current gain	296
BV_{EBO} [V]	0.95
BV_{CBO} [V]	10.7
BV_{CEO} [V]	3.5
R_C [Ω]	61
R_E [Ω]	30
f_T [GHz]	41
f_{max} [GHz]	42

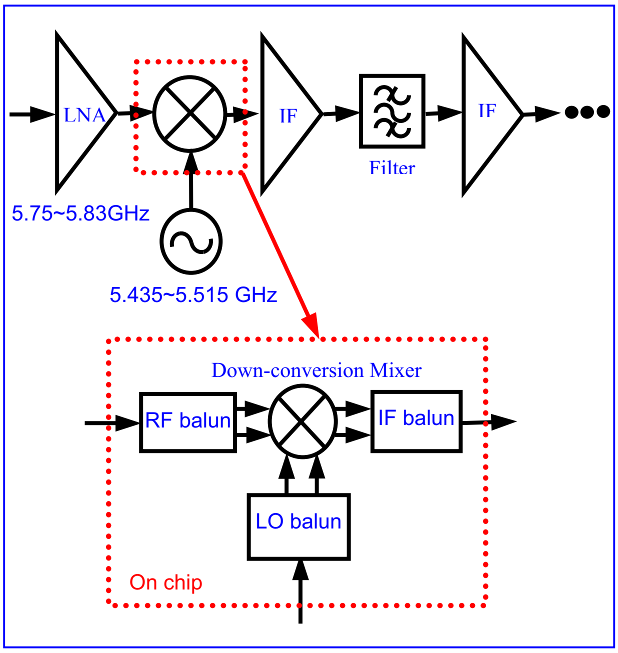

Fig. 2. Architecture of DRSC RF receiver and mixer

Fig. 4 shows a push-pull balun which is composed of a common-emitter with degeneration and the common-collector. The degeneration resistor R3 controls the gain of the common emitter path for the same amount of gain for both inverting and non-inverting signals, resulting in maximum cancellation of LO leakage at the output of the balun. R4 is included for output impedance matching. The gain of the balun is the sum of the two signal path gains [5]. The common-collector path provides highly linear performance and the common-emitter is more linear than the differential-pair for the same bias current and transconductance [4].

The above baluns are deigned and all integrated on chip together with mixer core circuit and provide good isolation.

Double-balanced bipolar mixer in the form of Gilbert cell used in this paper is shown in Fig. 5, which is differential structure to avoid the common-mode noise. When the switching transistors of the Gilbert cell mixer are driven fully differentially, theoretically, there is no LO leakage at the output. The emitter inductive degeneration (L3, L4) is also added to improve linearity.

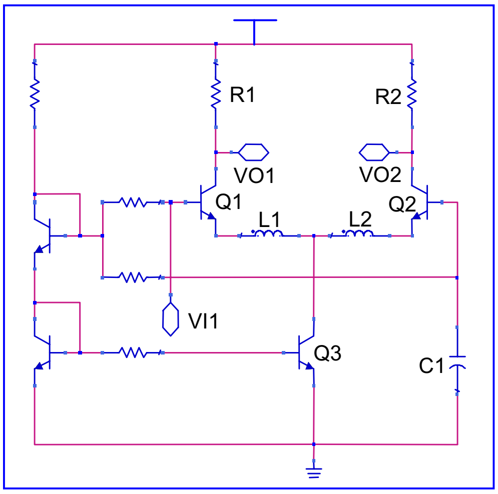

Fig. 3. RF/LO input balun with bias circuit

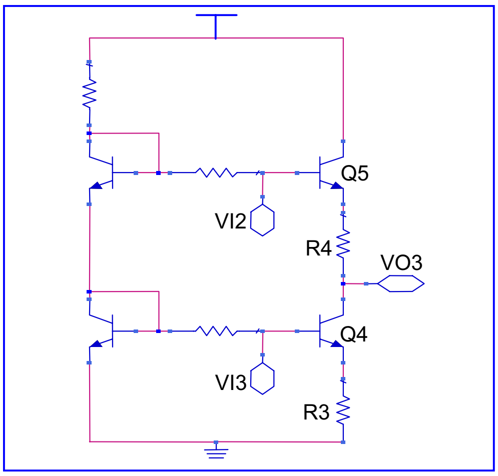

Fig. 4. IF output balun with bias circuit

IV. FABRICATION AND MEASUREMENTS

We designed and fabricated the mixer circuit using 0.8 μm SiGe HBT process technology. The manufactured mixer photograph is shown in Fig. 6 and this chip size is 1.9 mm × 1.3 mm. In Fig. 6, the upper pad is for supply voltage. The left, lower and right center pads are LO input, RF input, IF output pads, respectively.

For this measurement, two RF power sources HP83650B, HP83752B, and a spectrum analyzer HP8563E were used. The measurement conditions of the fabricated mixer were RF=-30 dBm, LO=-5.0 dBm, VCC=3.0 V (with local biases VA=3.0 and VB=2.5). Fig.

7 shows the measured frequency spectrum at IF output port (upper figure: 50 MHz~8.0 GHz range, lower figure: 100 MHz span) and conversion gain is 7.5 dB, LO to RF port-to-port isolation is 46 dB, LO to IF port-to-port isolation is 56 dB. Fig. 8 shows the measured IP3 when the LO input power was fixed to -5.0 dBm and the RF input power was swept from –30 dBm to –3 dBm and from this figure, IIP3 is –2.5 dBm. Table 2 shows comparison of the simulated and measured results.

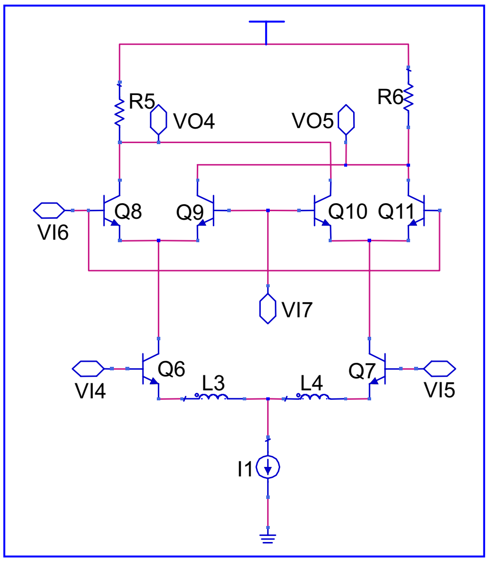

Fig. 5. Mixer with emitter inductive degeneration

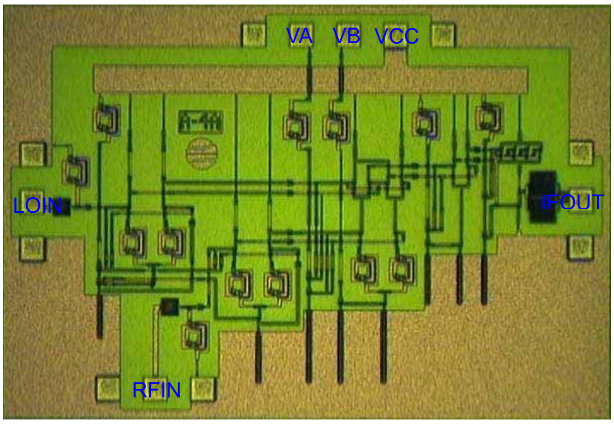

Fig. 6. Photograph of the fabricated mixer

Table 2. The performance of fabricated mixer

Parameters	Simulated	Measured
RF frequency [GHz]	5.810	5.810
LO frequency [GHz]	5.495	5.495
Conversion gain [dB]	8.0	7.5
LO to RF isolation [dB]	68	46
LO to IF isolation [dB]	43	56
RF to LO isolation [dB]	56	34
RF to IF isolation [dB]	40	30
IIP3 [dBm]	1.5	-2.5
IC [mA]	20	21

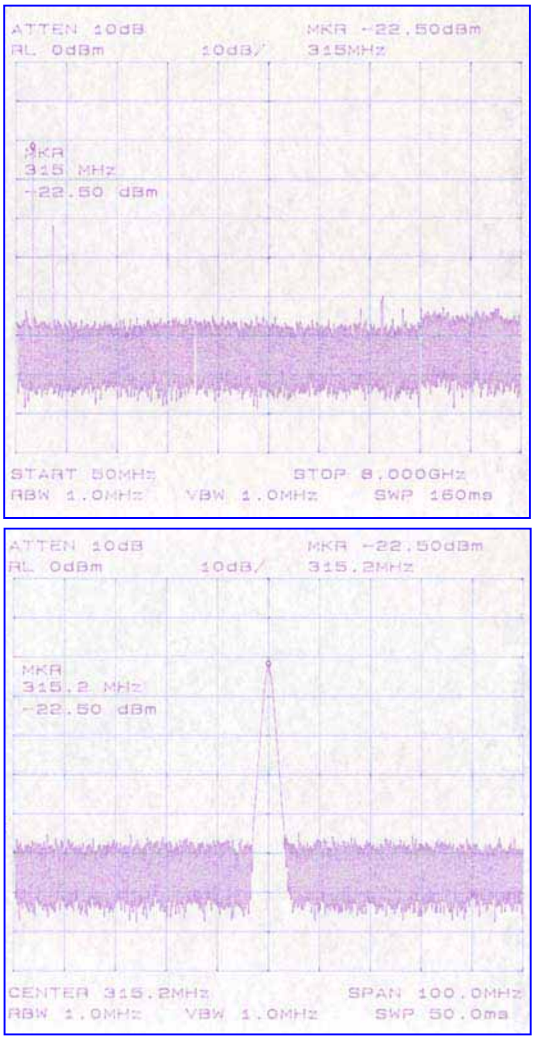

Fig. 7. The measured frequency spectrum at IF port (upper: 50 MHz~8.0 GHz range, lower: 100 MHz span)

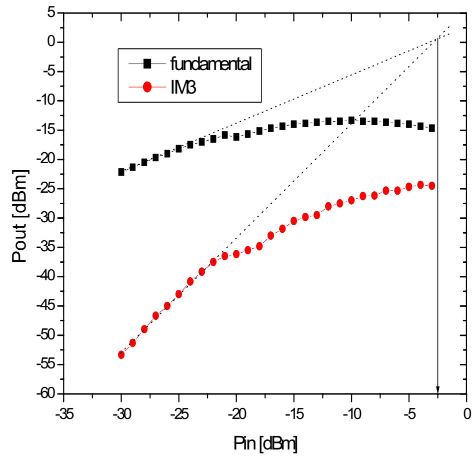

Fig. 8. The measured IP3 characteristics

V. CONCLUSION

DSRC provides high speed radio link between Road Side Equipment (RSE) and On-Board Equipment (OBE) within the narrow communication area and most of all ITS services will be provided by DSRC communication. In this paper, a 5.8GHz down-conversion mixer for

DSRC receiver was designed and fabricated using 0.8 μm SiGe HBT process technology and RF/LO matching circuits, RF/LO input balun circuits and IF output balun circuit were all integrated on chip. The measured performance was 7.5 dB conversion power gain, -2.5 dBm input IP3, 46 dB LO to RF isolation, 56 dB LO to IF isolation, current consumption of 21 mA for 3.0 V supply voltage.

ACKNOWLEDGMENTS

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