Novel Variable Attenuator pHEMT MMIC's for Millimetre Wave Radio Applications

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Variable attenuator circuits are essential system blocks in millimetre wave radio links. Two novel variable attenuator MMICs have been realized and tested: One with continuous i.e. analog control (VVA) and the other with three bit digital control (DA). Circuits operate in a very broad frequency range of 15 GHz – 45 GHz and they have been fabricated with commercially available GaAs pHEMT processes: VVA utilizing OMMIC 0.2 µm process and DA with TriQuint 0.25 µm process. The digital attenuator circuit reached an input 1 dB compression (or expansion) point of + 16 dBm at all attenuation states and an extremely low minimum insertion loss of 0.9 dB at 15 GHz and 2.5 dB at 45GHz. The dynamic range of attenuation was 35 dB at 40 GHz. The input 1 dB compression point of the voltage variable attenuator circuit was better than + 13 dBm at all levels of attenuation.

INTRODUCTION

Variable attenuators are widely used for automatic gain control in transceivers of microwave and millimetre wave radios. High linearity and low losses in variable attenuators are important features in order to keep the structure of the microwave unit of the transceiver simple and to maintain high linearity as well as good noise performance.

The linearity of a VVA (voltage variable attenuator) is typically high if the attenuator is at the minimum or at the maximum attenuation level. Between those levels the linearity is much lower. Digital attenuator offers high linearity at all states of attenuation.

Traditionally microwave radios, e.g. reported by Louhi et al (1), have been point-to-point radios with continuous data flow, which has prevented the utilization of digital attenuators due to the abrupt change of gain during switching of the attenuator state. The new packet mode radios standardized in ETSI EN 301785, ETSI HiperAccess and IEEE 802.16 enable gain controlling during idle time, which enables the usage of digital attenuators in those applications.

Digital attenuator offers high linearity combined with easy and accurate control of the level of attenuation over MMIC process variations and ambient temperature changes. Performances of typical digital attenuator designs from the literature are shown in Fig. 1. (2-6).

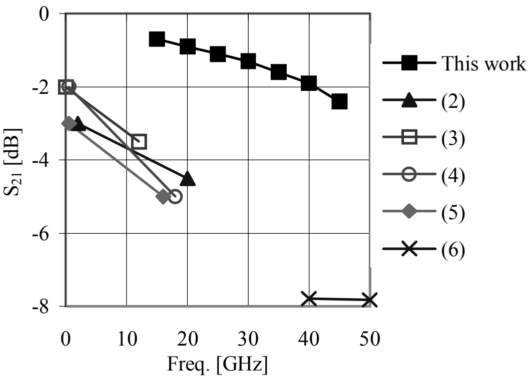

Figure 1: Comparison of insertion loss at the reference state of the reported digital attenuators.

The approaches of these designs are binary weighed “Pi” or “Tee” resistive networks with SPDT switches or designs containing switching FETs inside the “Pi” or “Tee” type resistive attenuator cells. These approaches are not well suited for low loss designs above 20 GHz where especially low insertion loss is required.

Chip size is a critical factor when a low cost design is pursued. The chip area of this work is as small as 1.5 mm^2. In contrast, the size of the chip of the low phase error 44 GHz attenuator is 10 mm^2 (6). The constant phase property of this design is not necessarily needed in typical transceivers in telecommunication radio link applications.

Typical non-reflective VVA circuit topologies at millimetre wave frequencies are “Tee” type, e.g. Alpha (7), and balanced type. “Tee” type VVA is small but it contains different control signals for series and shunt elements, which complicates the control of the VVA when appropriate input and output return losses should be maintained at all levels of attenuation. Both of the control voltages should track over process and temperature variations. Balanced type VVA occupies practically more than double of the chip area compared to a single-ended one, which increases the cost of the component.

This paper presents the design and measured results of a 3-bit digital attenuator and a voltage variable attenuator using a new circuit topology suitable especially for telecommunications applications at microwave and millimetre wave frequencies. The attenuators of this work are easy to control and they have also potential for multifunction MMICs by integrating the attenuator with e.g. amplifiers and mixers onto the same chip.

ATTENUATOR DESIGNS

Digital attenuator

The schematic and the photograph of the 3-bit digital attenuator are shown in Fig. 2 and Fig. 3. The device consists of three attenuation sections of 5 dB, 10 dB and 20 dB, respectively, and provides 35 dB dynamic range of attenuation. Each section utilizes a novel ”all-shunt” circuit topology in which pHEMTs are connected only in shunt and microstrip lines in series along the signal path. There are no pHEMTs connected in series, which is one key issue for the low loss of the attenuator. Namely, at high frequencies there is a significant trade-off between the “on” resistance and the isolation at the “off” state caused by parasitic drain to source capacitance Cds of the pHEMT. For low losses the “on” resistance should be as small as possible leading to a large size pHEMT and therefore large Cds.

The 20 dB section consists of two inductive microstrip lines TL1 and TL2 and three shunt pHEMT structures Q1-Q3, each containing two 1-finger pHEMTs connected in series. At minimum attenuation state input and output matches are provided by the inductive transmission lines TL1 and TL2, which compensates the parasitic capacitances of the pHEMTs Q1 - Q3. At the maximum attenuation state the resistance of the pHEMT Q2 is 16 ohms. This impedance is transformed by TL1 into a high impedance value, which is in parallel with the input pHEMT Q1 in order to form input impedance close to 50 ohm also at the maximum attenuation state. This is a straightforward way of getting non-reflective variable attenuation with very small losses. The 5 dB and 10 dB sections have only two shunt elements. Thin film resistors are avoided in the shunt elements in order to reduce losses. This may increase the tolerances of the attenuation because the value of the shunt resistance is based only on the drain to source resistance Rds of the pHEMT.

The circuit was simulated with HP EEsof Series IV simulation software using the models available from TriQuint. Electromagnetic simulations were carried out using Agilent Momentum simulator. The goal for return losses was 10 dB in frequency range of 20 GHz to 45 GHz at all attenuation states. There were only linear switch models available for the pHEMTs and therefore nonlinear properties of the digital attenuator were not simulated.

Voltage variable attenuator

The operating principle of maintaining good input and output return loss values at all levels of attenuation is the same as in digital attenuator design. The VVA contains two attenuator stages. The first stage has high linearity: input –1 dB gain compression point P_{-1dB} > 13 dBm at all levels of attenuation and 13 dB dynamic range of attenuation. The second stage has poorer linearity: P_{-1dB} > -2 dBm at 3 dB level of attenuation, but at the level of minimum attenuation the linearity is high: P_{-1dB} > 15 dBm. The dynamic range of the second stage is 30 dB. The schematic and the photograph of the VVA are presented in Fig. 4 and Fig. 5.

By sequential control of the voltages V_{ctrl1} and V_{ctrl2} the linearity at the input port of the VVA is high: P_{-1dB} > 13 dBm at all levels of attenuation. The second stage is kept at the level of minimum attenuation until the first stage is set to the maximum level of attenuation.

The high linearity of the first stage is achieved by stacking four 1-finger pHEMTs in series in each of the shunt elements. The second stage has only single pHEMTs in the shunt elements.

The circuit was simulated with HP Eesof Series IV simulation software using linear and non-linear models available from OMMIC.

MEASURED RESULTS

The attenuator chips were measured using Cascade probe station with RF probes from Picoprobe and Agilent HP8510C vector network analyzer. An additional amplifier was used in AM/AM and AM/PM conversion measurements.

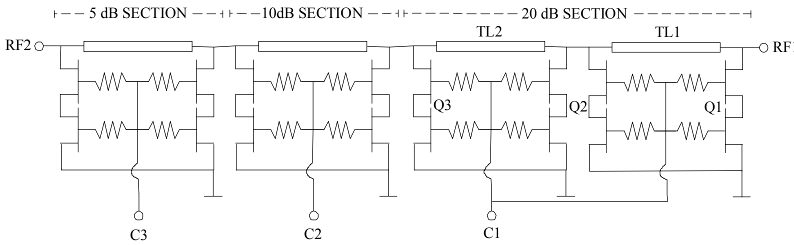

Figure 2: Schematic of the 3-bit digital attenuator comprising three sections of 5, 10 and 20 dB.

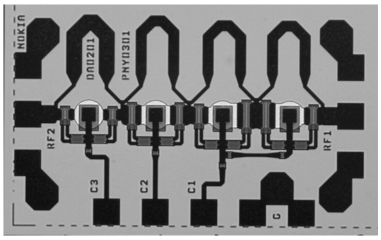

Figure 3: Photograph of the 3-bit digital attenuator. The size of the chip is 1.5 x 0.9 mm².

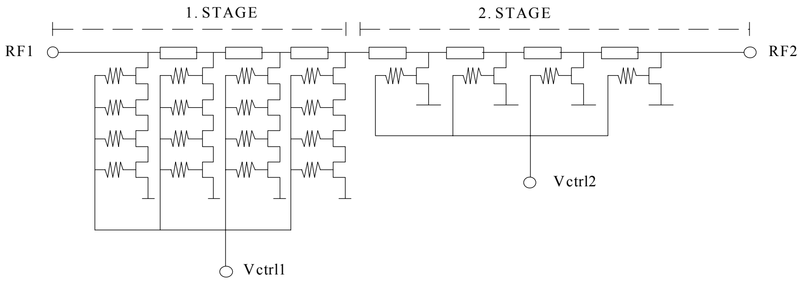

Figure 4: Schematic of the voltage variable attenuator. The first stage is controlled with voltage Vctrl1 and the second one with Vctrl2.

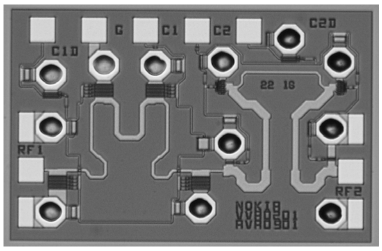

Figure 5: Photograph of the voltage variable attenuator. The size of the chip is 1.5 x 1.0 mm²

The measured performances of both of the attenuator chips are summarized in table 1.

Table 1
Measured performances of the digital attenuator and voltage variable attenuator chips

	DA	VVA	Unit
Frequency range	20 - 45	20 - 45	GHz
Minimum attenuation	< 2.5	< 3.3	dB
Dynamic range	34	38	dB
AM/AM: Input P_{-1dB} (at any attn. value)	> +16	> +13	dBm
|AM/PM at P_{-1dB}|	< 2	< 1	deg
Input and output return loss (at any attn. value)	> 7	> 7	dB
Chip size	1.4	1.5	mm²

Digital attenuator

Linear measurement results are presented in Fig. 6. Minimum insertion loss is 0.9 dB at 15 GHz and 2.5 dB at 45GHz. The dynamic range of the attenuation is more than 35 dB at 40 GHz. These results were in good agreement with the simulated ones. The input and output matching is 7 dB in the frequency range of 15 GHz to 45 GHz, which is 3 dB worse than simulated. A second iteration of the chip design is needed in order to meet the 10 dB return loss requirement.

The measurement results of the AM/AM conversion at 26.5 GHz are presented in Fig. 7. The +1 dB gain expansion point of the circuit is 16 dBm, in which the AM/PM conversion is -2 deg. The positive AM/AM and negative AM/PM conversion properties of the device indicates that the 5 dB section of the attenuator also has potential as an RF pre-distortion linearizer for power amplifiers which have positive AM/PM conversion characteristics.

Voltage variable attenuator

Minimum insertion loss of the VVA is 2 dB at 20 GHz and 3 dB at 40GHz. Dynamic range is 42 dB and 47 dB at the same frequency points. Input and output matching is better than 7 dB at a frequency range of 20 - 45 GHz at all levels of attenuation.

The measured data of AM/AM conversion at 26.5 GHz is presented in Fig. 8 and 9. The 1 dB gain compression point is better than +13 dBm at all levels of attenuation. AM/PM conversion is less than +1 deg at 1 dB gain compression point. There is gain expansion at high power levels, when the first stage is at maximum attenuation state. This phenomenon compensates a part of the gain compression of the second stage and its linearity performance can be worse than in the first stage.

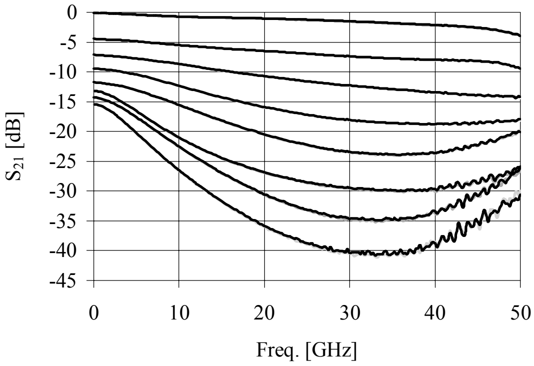

Figure 6: Attenuation vs. frequency of two measured 3-bit attenuator MMICs at all of the eight attenuation states. The top curve represents the reference level and the bottom curve is the maximum level of attenuation. The size of the step is 5 dB.

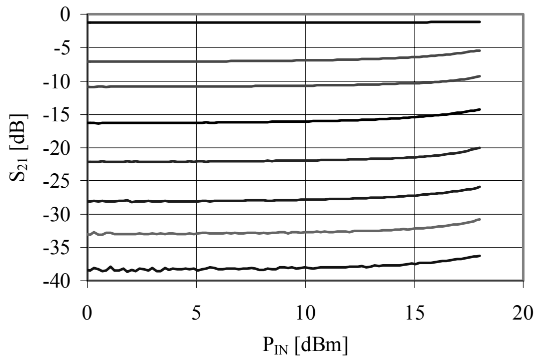

Figure 7: AM/AM conversion of the 3-bit attenuator MMIC at 26.5 GHz at all of the eight possible attenuation states.

CONCLUSION

A high linearity digital attenuator and a voltage variable attenuator MMICs were designed, fabricated and tested. The circuits achieved very low insertion losses at minimum attenuation level in a broad band (20 GHz to 45 GHz). Typical pHEMT processes were used, so the circuits can be integrated with other functions onto the same multifunction MMIC. These properties together with the small size of the design (1.5 mm^2) are important for low cost radios operating at microwave and millimetre wave frequencies. Patent pending.

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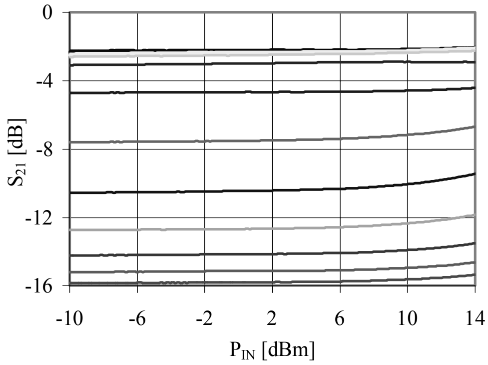

Figure 8: AM/AM conversion of the voltage variable attenuator at 26.5 GHz. The first attenuator stage is controlled from minimum to maximum level of attenuation. Vctrl1 is controlled from -2 to 0 V and Vctrl2 is constant –2 V.

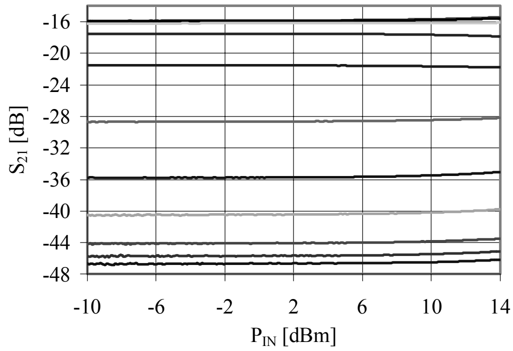

Figure 9: AM/AM conversion of the voltage variable attenuator at 26.5 GHz. The second attenuator stage is controlled from minimum to maximum level of attenuation. Vctrl1 is constant 0 V and Vctrl2 is controlled from -2 to 0 V.

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