Process-Tolerant High Linearity MMIC Power Amplifiers

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Abstract — **The success of an MMIC design is strongly influenced by the process tolerances and model inaccuracies. In fact the MMIC technology is tuneless and all the problems related to the component tolerances must be taken into account in the design phase. This issue is even more relevant in high linearity power amplifiers. In this kind of devices many different parameters (P1dB, PAE, C/I) shall be simultaneously optimized, and, if not properly taken into account, process tolerances may affect the device performances, compromising the fulfillment of the desired requirements.**

In this paper the most relevant uncertainty sources and the factors influencing the process tolerances will be analyzed, giving the guidelines to keep under control the effect of process variation parameters and model inaccuracies.

I. Introduction

MMIC technology is well recognized as a cost effective solution for a number of applications (digital radio, LMDS, VSAT) in the millimeter-wave frequency range, also allowing a reduction in size, weight and complexity of systems. In modern multi-channel high capacity communication systems, when dealing with high spectral efficiency modulation schemes, there is a stringent requirement to minimize interference to adjacent channels, in order to avoid data loss. At a circuit level this issue can be addressed improving the trade-off between linearity and power added efficiency in the output stage power amplifiers.

In general, the design of a highly linear power amplifier implies that the output terminations of the active components must be chosen with a great accuracy in a relatively small region of the Smith chart. If not properly taken into account, process related tolerances and inaccuracies in passive and active element models can shift the real load experienced by the active device causing a drastic worsening of the device performances. Due to the tuneless nature of MMIC technology, a possible load shift would lead to a complete re-design of the device without the possibility to correct the design inaccuracies after the test phase. For all these reasons in MMIC highly linear power amplifiers the exact knowledge of the process tolerances and the inaccuracy of the models used in the circuit simulations are critical aspects.

II. Inaccuracy Sources

An MMIC designer would willingly deal with component models with infinite precision in all the frequency range and with a manufacturing process unaffected by tolerances and spread in physical and electrical parameters. Unfortunately in the real world this is not the case. The electrical models of real components have a finite accuracy that generally decreases with increasing frequency and any fabrication process has its own tolerances. However a process tolerant design must provide a device compliant with the given requirements despite any kind of dispersion or inaccuracy.

Although both problems can lead to the same result (the simulated response different to the real circuit performance), model inaccuracies and process tolerances are two distinct sources of error and the actions to be taken in order to reduce their impact on the final design are different. Moreover, it can happen that their entity is of the same order of magnitude. In those cases it is not trivial to evaluate how to combine the two error sources and which is the overall tolerance the designer have to consider.

A. Process Tolerances

Each fabrication process has an intrinsic finite precision. Substrate height, thickness of the various metallic and dielectric layers, geometry definition, via hole diameters are all parameters that can be defined within some tolerance range. The spread in a given range of the component physical parameters will lead to a statistical distribution of its electrical performances. This kind of errors is generally expressed by manufacturers as a few percent tolerance over the electrical parameters. Note that very often a uniform tolerance may represent an approximation. Consider for instance a MIM capacitor, square shaped, and assume the capacitance C equal to

$$C = \frac{\varepsilon\, l^2}{d} \tag{1}$$

with ε taking also the leakage effects into account, l being the capacitance plate side and d the dielectric thickness. If we call σ_A the standard deviation of the generic parameter A ($A = l,\ d,\ \varepsilon$) and we assume all

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statistical distributions as Gaussian and without correlation, we obtain

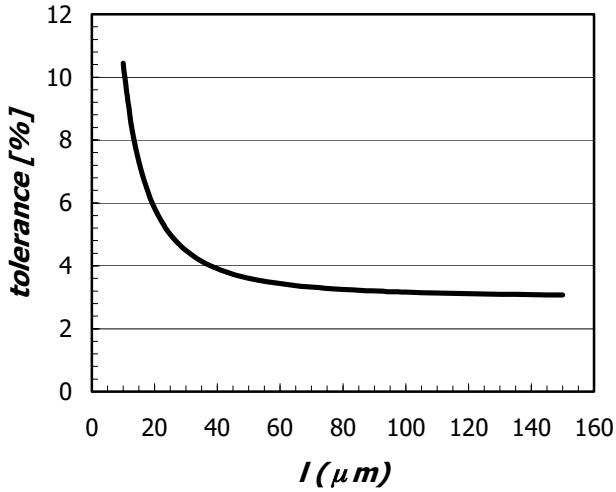

Fig. 1. σ_C/C as a function of the capacitor side dimension, assuming the residual tolerance due to the dielectric thickness and permittivity as equal to 3%, and the side length dispersion within 0.5 μm.

$$\frac{\sigma_C}{C} = \sqrt{\frac{4\sigma_l^2}{l^2} + \frac{\sigma_d^2}{d^2} + \frac{\sigma_\varepsilon^2}{\varepsilon^2}} \qquad (2)$$

From (2) it is easy to note that if the absolute error on the cap plate side is constant (σ_l = 0.5 μm), the cap tolerance (σ_C/C) increases as the cap size decreases. Moreover σ_C/C is independent of the cap value only if we can neglect the error on the cap side ($\sigma_l/l << \sigma_d/d$, $\sigma_\varepsilon/\varepsilon$). In fig. 1 σ_C/C is represented as a function of the cap plate side l, assuming σ_l = 0.5 μm and $\sqrt{\frac{\sigma_d^2}{d^2} + \frac{\sigma_\varepsilon^2}{\varepsilon^2}} = 0.03$.

B. Model Inaccuracies

Chip manufacturers generally provide the designers with their own model libraries. Models should give the exact electrical response of the active devices and all circuital elements used to design the matching networks. These models are usually valid in a finite frequency range and have a finite accuracy. Moreover, the electrical models of active devices (i.e. MESFET, PHEMT, etc.) also have some limitations as for the bias point and the power range. Also when used in their validity range, they will provide the exact electrical response within a certain accuracy (generally specified by the foundry). Compared to process tolerances this kind of errors is of a different nature, even if it induces on the circuit similar effects. In fact model inaccuracies are not statistical variables, leading either to an overestimation or to an underestimation of the component electrical parameters.

In general, it is not easy to quantify how good a model is, at least for two different reasons. The first one is that even the simplest component (let's say a capacitor or a resistor) is modeled with a complex network, in order to take all parasitic effects into account. This implies that a good model must provide not only the correct nominal value of the component, but more in general it should provide the complete S matrix as a function of the component geometry (node width, component nominal value, etc.) and frequency. Then a complete description of the model accuracy should be done analyzing the scattering matrix of the component for different parameter values.

The second reason is that it may happen that the accuracy may significantly change depending on which parameter is considered. For example, for nearly pure reactive elements with a negligible resistive component (inductances and capacitors) it often happens that a small error in the S parameters will produce a larger error on the Z or Y parameters (see fig. 2). This means that the model accuracy can be a function of the specific application in which it is used.

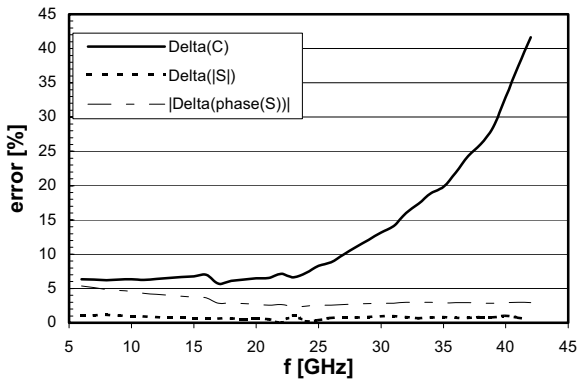

Fig. 2. Difference between measurement and model of a 0.2 shunt capacitor. Note that the error is very different, depending on which parameter is considered. Although the amplitude (short dashed line) and the phase (long dashed line) of $S_{1,1}$ have an error between 1 and 5%, the error on the capacitance value (straight line) raises up to 40%.

A robust design must take into account both the process tolerances and the model inaccuracies and the designed circuit has to properly work independently of how relevant they are.

If one of the two error sources is dominant, the sensitivity analysis is straightforward. Otherwise it is not obvious to understand how to combine the statistical errors with the model errors. Let's consider once again a capacitor. The statistical error, as given by the manufacturer, is in general expressed as a few percent tolerance on the capacitance value. As already remarked, the model accuracy should be expressed in terms of a set of complex parameters (i.e. S parameters). A way to approximately compare the two error sources is to evaluate the impact of the model S-parameter inaccuracies on the component nominal value. Expressing the model inaccuracy in terms of an error on the nominal capacitance value, it is possible to compare it to the standard deviation due to the manufacturing process. Note that summing the correction on the nominal value with the process tolerance on the capacitance can lead to an overestimation of the effective tolerance (see fig. 3). Of course a design that is tolerant to the sum of statistical error and model inaccuracy will be enough robust to work properly in the worst case

hypothesis, but it could be a very hard task to be obtained.

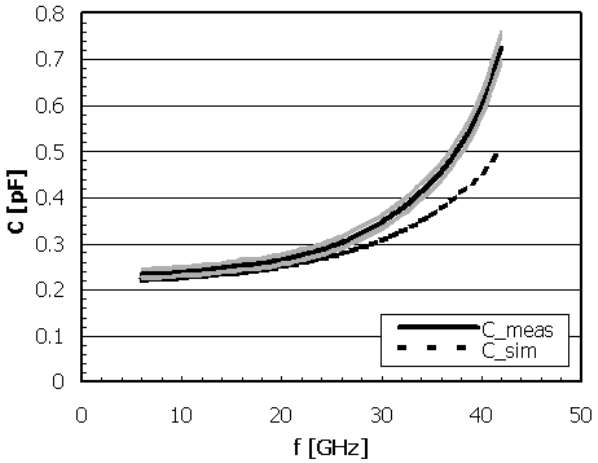

Fig. 3. Comparison between model and measurements for a 0.2 pF (nominal value) capacitor. The capacitor is assumed to have a 5% dispersion (gray band). The model (dashed line) underestimates the capacitance value and its inaccuracy increases as the frequency increases. Note also that approaching the resonance frequency the model becomes very inaccurate (up to 40% on the cap nominal value; see also fig. 2). Moreover it is clear from the graph that, by just summing the model inaccuracy and the manufactory dispersion, the total tolerance would be overestimated.

III. Process-Tolerant Design

There are many actions a designer can take in order to reduce the risks related to the different error sources discussed in the preceding section. To this aim it is possible to proceed in two different ways. On one hand you can try to reduce error sources, on the other you have to minimize the design sensitivity. Of course, the optimum solution would be doing both.

The only way to reduce the process tolerance is acting on the process itself, but this issue will not be under the designer's control. The only thing a designer can do is to take into account the process tolerances as a relevant aspect of the design, when choosing a specific technology, and eventually prefer a technology or a process variant able to reduce dispersion.

In order to reduce the model inaccuracies, it will be of some help to have the S parameter measurements of all the components the designer is going to use. In this way it is possible to correctly evaluate the different models accuracy and the "safety margin" needed in the design. Models given by foundries generally have to fit the real component in a wide frequency range and for different values of some geometric parameter. In order to improve their accuracy, a designer can think of optimizing the model in his frequency range of interest, and restricting the range of the geometric parameters.

In order to design a robust, process-tolerant, highly-linear power amplifier, we propose to adopt the following simple rules:

a) Choose the cell terminations not only as a trade-off between gain and linearity, but also as a trade-off between gain, linearity and sensitivity. In some cases it is better to choose a load that is not an optimum, if it will reduce the circuit sensitivity. In other words circuits have to properly work not only with the nominal loads but with all the loads within the possible range of variation. Note that errors in the active device model will lead to a bad estimation of the optimum load, whereas errors in the passive element models will lead to a difference between the simulated load and the load really experienced by the cell. In both cases the result is an output load different from the optimum.

In order to correctly evaluate the linear and non-linear cell performances, it is of primary importance to perform load-pull measurements in a wide region of the Smith chart. The same result can also be obtained if an accurate non-linear model is available.

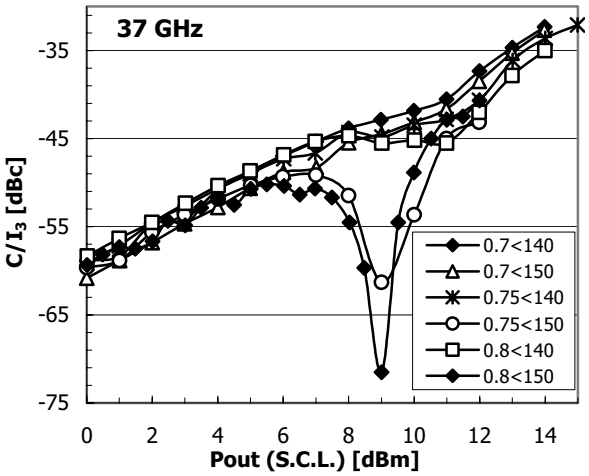

Fig. 4. IMD measurement on a GaAs 0.25 μm PHEMT as a function of the output power for different output terminations. Note the presence of a sweet spot for some values of the load. For higher values of the output power the slope of IMD increases up to 4 (if measured in dBc).

b) Avoid "sweet spots". In GaAs PHEMT it is common to measure a "sweet spot" in the third order intermodulation product curve [1]. Spots generally appear when two non-linearity sources are summed in phase opposition (input and output nonlinearities; 3rd and 5th order nonlinearities etc.) thus resulting a sharp minimum in C/I_3 vs P_{out} curve (fig. 4). Being this effect a perfect balance of two distortion sources, the exact notch position is very sensitive to input and output load, process tolerances, bias condition, temperature, harmonics termination, etc. For this reason trying to use this effect in order to reduce the overall IP3 performances is very risky. Moreover when the notch is due to a 3rd and 5th order effect compensation, IMD3 of the circuit rapidly degrades for output power higher than the notch (IMD3 will raise as P^5). Designing "far from the spot" will be safer and although the circuit will decrease its performances, it will gain in robustness.

c) Avoid using components with a high dispersion. For example, as already remarked, small capacitors are more dispersed than larger capacitor. As it can be seen in

fig. 1, tolerance on the capacitance value will decrease with an l^{-1} law, l being the capacitor plate side. Moreover, shunt capacitors suffer also from a relevant dispersion in the inductance value related to the via hole. When dealing with such components accurately consider where the resonance frequency is and avoid having it near the frequency range of interest.

d) Avoid circuit topologies sensitive to a single element, above all if the component model is inaccurate or if it is a component with high dispersion.

e) Avoid using sharp resonances to equalize the frequency band nor to design a matching network. In presence of a resonance, the greater is Q, the higher is the network sensitivity.

f) When possible use microstrip structures electromagnetically simulated. In general electromagnetic simulations are more accurate than electric models and with an extensive use of electromagnetic simulation it is also possible to take into account the coupling of different parts of a network. Remember also that an open stub (shorter than $\lambda/4$) can act as a shunt capacitor and a series capacitor can be easily done with interdigit technology. These are two common examples of lumped components made with microstrip structures.

g) Design networks with a geometry easy to be (electromagnetically) simulated. Avoid uncalibrated ports. Avoid unwanted coupling effects. Use an appropriate circuit meshing.

Device Name	**PA13-15**	**PA28-32**	**PA37-40**
Freq. band [GHz]	12.7-15.4	27.5-32.5	36.5-40.5
Linear gain [dB]	15	16	14
Input RL [dB]	19	19	19
Output RL [dB]	19	19	19
P_{1dB} [dBm]	28	28	28
IP_3 [dBm]	38.5	38.5	37.5
P_{DC} [W]	3	3.5	6.4

TABLE I
PAXX-XX AMPLIFIER FAMILY PERFORMANCES

PAXX-XX: HIGHLY LINEAR POWER AMPLIFIER FAMILY

Following the procedure described in a preceding paper [2] and the prescriptions reported above, a new GaAs MMIC power amplifier family was designed. The amplifiers cover the main frequency ranges from 12.5 GHz up to 40 GHz. The main electrical amplifier performances are summarized in tab. 1. The technology selected was GaAs 0.25 μm power PHEMT – 3 Metal Interconnect. A process variant with higher linear performances and a lower dispersion was used. For each amplifier of the family the PHEMT geometry and the cell terminations were chosen after an extensive linear and nonlinear characterization (load pull) by means of directly on-chip measurements. The non-linear cell characterization was completed by means of a suitable non-linear model [3]-[4]. Both active and passive component models were validated by means of S-parameter measurements. In order to further reduce the sensitivity to manufacturing process dispersion and to increase the return loss performances, a balanced configuration based on Lange couplers was adopted.

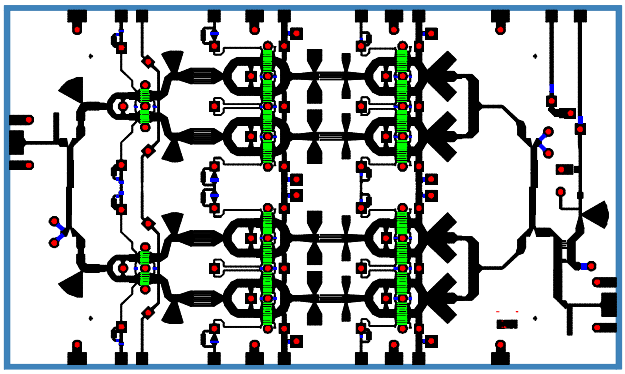

Fig. 4. Layout of PA37-40. Note the wise use of many microstrip structures in substitution of lumped components.

CONCLUSIONS

The issues related to the tolerance process and model accuracy are a relevant topic in a circuit design. These topics are even more important if an MMIC technology is adopted, because of the tuneless nature of a monolithic circuit. For a process-tolerant design it is important to consider tolerance and accuracy issues from the beginning and the specific technology and the circuit topology must be chosen taking into account the sensitivity of the circuit to these error sources.

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REFERENCES

[1] M. Pagani, D. Argento, M. Bignamini, I. De Francesco, G. Favre, A. Meazza, A. Mornata, and F. Palomba, "Characterisation of PHEMT intermodulation behaviour for highly linear MMIC power amplifier design", in *Proceedings of the 32nd European Microwave Conference (GAAS 2002)*, Milan, Italy, September 2002, pp. 355-358.

[2] M. Bignamini, G. Favre, A. Meazza, M. Pagani, F. Palomba, and G. Sivverini, "Efficient development of highly linear MMIC power amplifier", in *Proceedings of the 31st European Microwave Conference (GAAS 2001)*, London, UK, September 2001, pp.693-696.

[3] F. Filicori, G. Vannini, A. Santarelli, "A finite-memory nonlinear model for microwave electron device", in *Proceedings of the 5th European Gallium Arsenide and related III-V compounds Application Symposium*, Bologna, Italy, September 1997, pp. 83-86.

[4] A. Costantini, R. P. Paganelli, P. A. Traverso, D. Argento, G. Favre, M. Pagani, A. Santarelli, G. Vannini, and F. Filicori, "Accurate prediction of PHEMT intermodulation distortion using the nonlinear discrete convolution model", in *Proceedings of MTT-S International 2002*, Vol. 2, pp. 857-860, Washington, USA, June 2002.