Electrothermal and trapping effects characterisation of AlGaN/GaN HEMTs

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***Abstract* — This paper presents a systematic analysis of the two kinds of traps encountered in AlGaN/GaN HEMTs. It is shown that passivation is very efficient to minimize the surface trap effects but has little effect on the buffer traps. Those ones can only be eliminated through the development of high purity substrates. Moreover thermal I-V and microwave behaviour of such transmissions is investigated through the use of a pulse-measurement system.**

I. Introduction

Wide band-gap transistor technologies such as AlGaN/GaN HEMTs are very promising for radio frequency and microwave power generation [1]. Indeed they present high breakdown voltages as well as high current densities. Moreover they can also work at high temperatures. However, parasitic effects induced by trapping phenomena severely limit the power performances of these transistors [2], [3].

Pulsed I.V. measurements have demonstrated their usefulness for characterising such trapping behaviour [4]. In this paper we show that two kinds of measurements allow to discriminate the two kinds of traps that can be encountered in AlGaN/GaN devices: surface traps and buffer or substrate traps. Effects corresponding to the former type can be minimised by passivation techniques while the latter are much more difficult to eliminate. Measurements of 2x50 µm AlGaN/GaN transistors grown on various substrates have been carried out and compared.

Moreover thermal behaviour of such transistors is of prime importance due to the high power densities that can be reached. Temperature dependent pulsed measurements allow to derive electro-thermal characteristics of these transistors.

II. Trapping Effects Characterisation

The trapping effects correspond to the existence of energy states which can be occupied by holes or electrons in the gap. These holes or electrons are then maintained in these levels during an important lapse of time and cannot take part in the conduction, hence the term 'trap'. They generally result in the presence of impurities or defects in the crystalline network of the material they are composed of. These phenomena alter the electric behaviour of the transistor at microwave frequencies.

In order to determine the trapping effects thanks to the pulse measurement, we must establish a rigorous measuring protocol so as to differentiate the surface trapping effects (gate-lag) and the buffer trappings (self-backgating) as accurately as possible. First of all it is necessary to make sure that the duration of the pulses is lower than the emission time constant of the traps. Thus we chose a pulse duration equivalent to 400 ns with a recurrence equal to 6µs. Finally, to make sure that the differences recorded in the measures are those coming from trapping effects, we must work with a constant temperature, hence with a constant dissipated power.

The two kinds of ionised traps are figured at Fig. 1. Surface traps results from deep level acceptors that are ionised when the gate voltage is set below pinch-off [5]. Buffer or substrate traps are localised near the channel and are ionised when an electric field is set up in the channel direction resulting from a Vds voltage different from zero.

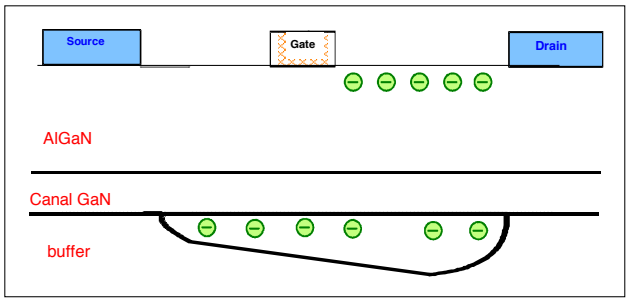

Fig. 1. Localisation of trap effects

A. Characterisation Of Gate-Lag Phenomenon

The 'gate-lag' phenomenon is mainly attributed to surface trapping effects. To determine these surface trapping effects, we make two series of pulse measurements with an identical dissipated power (P_{diss} = 0W). For that, we choose two quiescent biases equivalent to (Fig. 2) :

$$Vgs_0 = Vp,\ Vds_0 = 0V \quad (1)$$

$$Vgs_0 = 0V,\ Vds_0 = 0V \quad (2)$$

Therefore we can say that in both cases we work with an identical power equivalent to zero**;** consequently a difference between both I(V) characteristics implies the presence of gate-lags.

In this case as the quiescent Drain voltage is equal to zero, we can make the assumption that the number of ionised buffer traps is low.

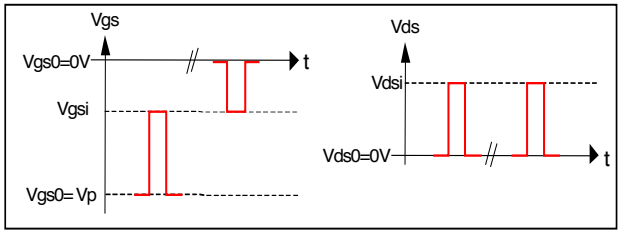

Fig. 2. Method of measurement to determine the gate-lag effects

We apply the measurement method described at Fig.2 to two AlGaN/GaN 2x50 µm transistors on SiC substrate. The difference between these two transistors is that one of them is passivated and the other one is not (Fig. 3). To realise the measures, we bias the passivated transistor, using two different quiescent biases :

$Vgs_0 = -7V$, $Vds_0 = 0V$

$Vgs_0 = 0V$, $Vds_0 = 0V$

with a $-7V \le Vgs_i \le 2V$ by step of 1V.

Then we bias the second transistor (which has not been passivated) with, again, two different quiescent biases :

$Vgs_0 = -3V$, $Vds_0 = 0V$

$Vgs_0 = 0V$, $Vds_0 = 0V$

with a $-3V \le Vgs_i \le 1.5V$ by step of 0.5V.

Consequently we work with $P_{diss} = 0W$.

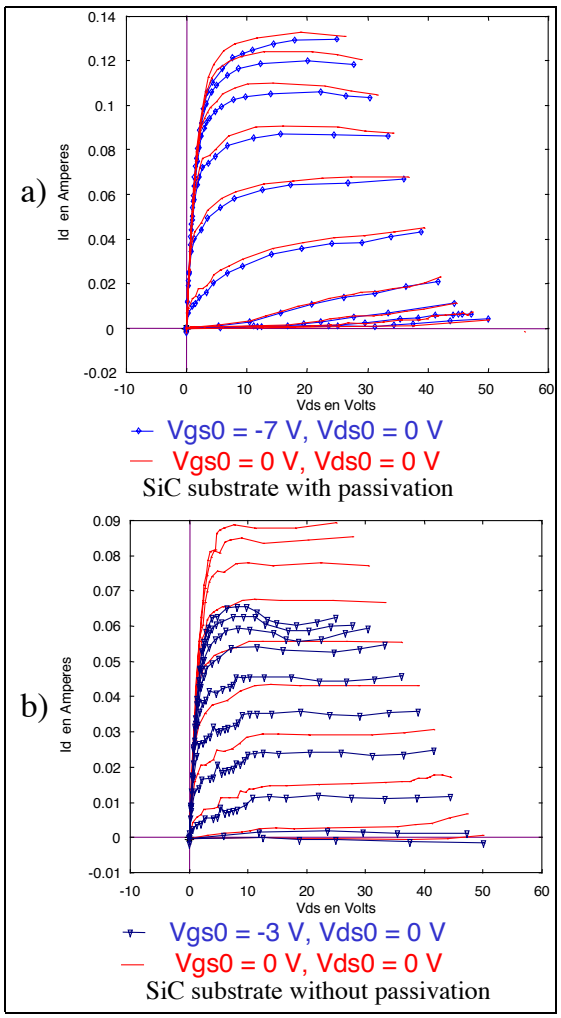

Fig. 3. Output I(V) characteristic for AlGaN/GaN 2x50 HEMTs grown on SiC substrate **a)** with passivation **b)** without passivation

We can notice that there is a strong decrease of drain current on the non-passivated transistor, whereas on the passivated transistor the output current decreases slightly.

However, even in this case of the strong decrease of the drain current, the knee-voltage of the HEMT is not modified by the quiescent gate bias.

As a consequence, the passivation is a good mean to limit the gate-lag effects.

B. Characterisation Of Self-Backgating Phenomenon

Just like the gate-lag phenomenon, the self-backgating phenomenon manifests itself through slow transient effects of the drain current , and therefore it creates a limitation of the output current especially for Vds voltages that are below the quiescent Drain voltage Vds_0. This effect is due to traps in the buffer. The self-backgating effects appears when the electrical field between the drain and the source increases suddenly.

Indeed, the electrons from the channel are injected in the buffer and are quickly trapped charging the buffer negatively. Thus this space charge region acts as a back-gate. Consequently in order to maintain the global neutrality, the electron sheet density in the channel decreases leading to a decrease of the drain current.

Just like before, in order to determine the self-backgating effects, we will make two series of pulse measurements with an identical dissipated power equal to zero. To achieve this, we choose two quiescent biases equal to (Fig. 4) :

$$Vgs_0 = Vp,\ Vds_0 = 0V \quad (3)$$

$$Vgs_0 = Vp,\ Vds_0 >> 0V \quad (4)$$

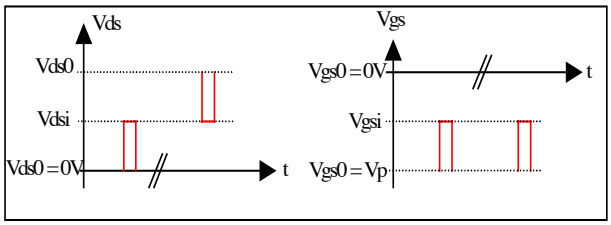

Fig. 4. Method of measurement to determine the self-backgating effects

We apply the measurement method described before to the same passivated transistor that was shown in Fig.3-a. To realize the measures, we bias this transistor, using two different quiescent biases :

$Vgs_0 = -7V$, $Vds_0 = 0V$

$Vgs_0 = 7V$, $Vds_0 = 25V$

with a $-7V \le Vgs_i \le 2V$ by step of 1V.

The quiescent gate bias was set to –7V and the characteristic shown in Fig. 5 exhibits a large increase of the knee voltage. This shows that despite a good passivation, there remains a reduction in the output power due to the presence of buffer traps.

Indeed applying a large electric field between drain and source leads to the ionization of a large number of traps that are located near the channel. It can be observed that above the quiescent drain bias, the characteristics are almost identical. This fact reveals that the number of

ionized traps depends on the maximum value of the bias voltage Vds_i rather than the average value Vds_0 [4].

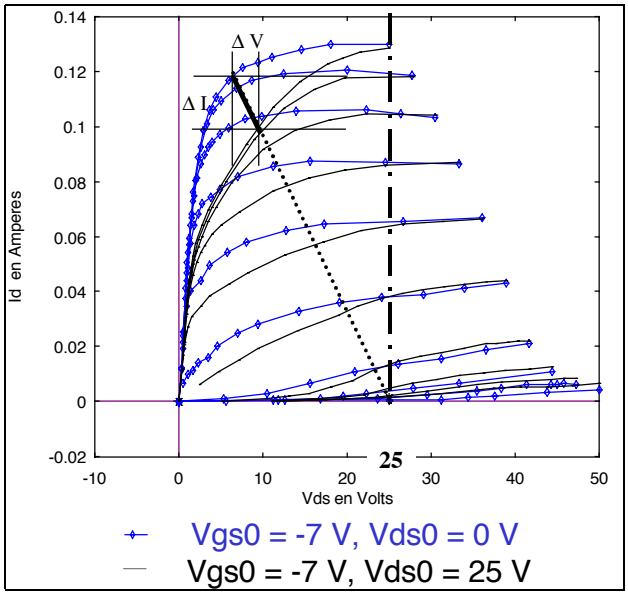

Fig. 5. Output I(V) characteristic for AlGaN/GaN 2x50 HEMTs grown on SiC substrate

This is due to the difference between the capture time constant and the emission time constant of the traps.

The same experiments have been performed on other transistors grown on sapphire and Si substrates. The transistor grown on sapphire was biased using two different quiescent biases (Fig. 6) :

$Vgs_0 = -5V$, $Vds_0 = 0V$

$Vgs_0 = 5V$, $Vds_0 = 20V$

with a $-5V \leq Vgs_i \leq 1V$ by step of 1V,

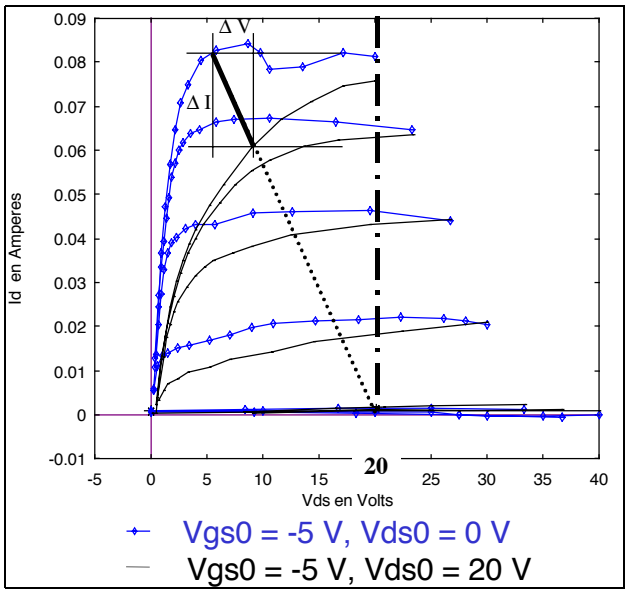

Fig. 6. Output I(V) characteristic for AlGaN/GaN 2x50 HEMTs grown on Sapphire substrate

and the transistor grown on Si was biased in the same way with (Fig. 7) :

$Vgs_0 = -6V$, $Vds_0 = 0V$

$Vgs_0 = 6V$, $Vds_0 = 20V$

with a $-6V \leq Vgs_i \leq 2V$ by step of 1V.

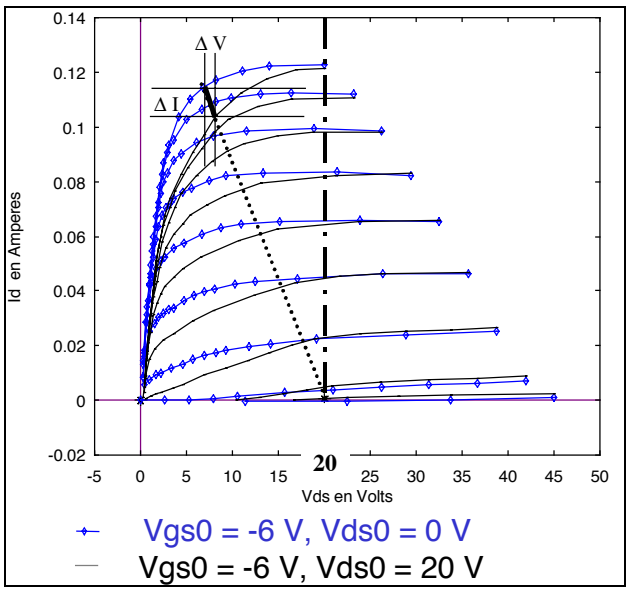

Fig. 7. Output I(V) characteristic for AlGaN/GaN 2x50 HEMTs grown on Si substrate

We can remark that whatever the nature of the substrate, the buffer trapping effects (self-backgating) are very present. As a matter of fact, we can see that the drain current is really affected by this bias change at dissipated power equal to zero.

The effects of traps can be evaluated by measuring the decrease of the maximum available drain current (ΔI) and the increase of the knee-drain voltage (ΔV). Those quantities are evaluated along an ideal load-line that provides the maximum of output power in a deep AB class / B class. Table I summarizes the results obtained.

AlGaN/GaN HEMT 2X50			
	SiC substrate	**Sapphire substrate**	**Si substrate**
ΔI (mA)	18.33	21.35	10.83
ΔV (V)	3.24	3.64	1.48

TABLE I
MEASURES OF VOLTAGE/CURRENT DIFFERENCES DUE TO DRAIN TRAPS ON DIFFERENT SUBSTRATES

As can be noticed from the previous figures, this modification of the output characteristics strongly affects the available output power as well as the power added efficiency.

III. ELECTRO-THERMAL CHARACTERISATION

Moreover our pulse-mode test bench allows us to realise electro-thermal measures (-65°C to +200°C).

We have made measures in pulses of the AlGaN/GaN 2x50µm transistor on SiC substrate from 22°C to 200°C for a quiescent bias in AB class ($Vgs_0 = -3.5V$, $Vds_0 = 24.5V$) (Fig. 8).

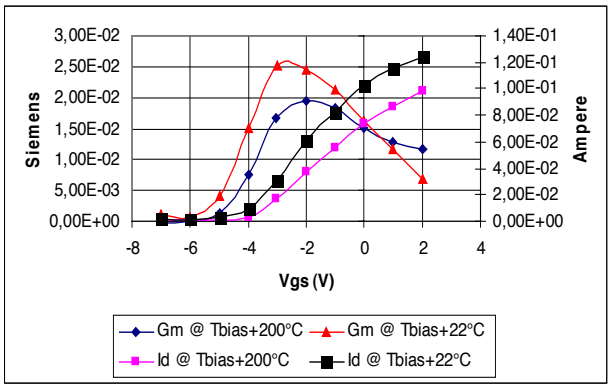

Fig. 8. Evolution of Id and Gm in function of Vgs for Vdsi=20V at T=Tbias+22°C and at T=Tbias+200°C.

We notice a decrease of the drain current and the maximum gain when the temperature increases; this is linked to a decrease of the electrons' mobility.

We also remark a significant decrease of the maximum gain when the temperature increases (Fig. 9). Moreover we notice a decrease of the maximum oscillating frequency when the temperature increases. On the other hand, the transition frequency remains almost constant (33 GHz), this is due to the decrease of the gate to source capacitance versus temperature.

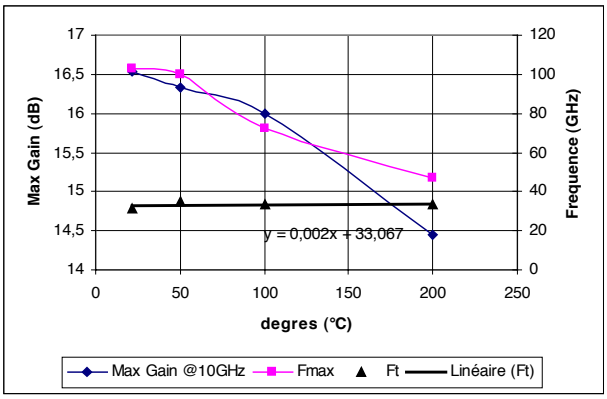

Fig. 9. Evolution of the maximum gain @10GHz, of the maximum oscillating frequency, and the transition frequency in function of the temperature.

VI. Conclusion

In short, throughout this study we can say that, thanks to (I(V) and [S]) pulse measurements and according to a specific measuring protocol, we noticed two things concerning the trapping effects:

- that passivation had a very beneficial effect on gate-lag effects
- that whatever the nature of the substrate is (SiC, sapphire, Si), the buffer trapping effects (self-backgating) are always present.

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