Novel compact double balanced coplanar active mixer
Application to a single chip MMIC receiver for satellite repeater

JF. VILLEMAZET, E. ROGEAUX, D. ROQUES,
JC. CAYROU, B. COGO, M. SOULARD, JL. CAZAUX

ALCATEL SPACE INDUSTRIES, 26 Av JF.Champollion, 31037 TOULOUSE Cedex, FRANCE
Jean-Francois.Villemazet@space.alcatel.fr

ABSTRACT

This paper proposes a new compact double balanced coplanar mixer suitable for satellite repeaters. Compared to the present 14/12GHz satellite mixers, its size is divided by 3 and it provides 2dB gain instead of the classical 10dB loss. This mixer was successfully integrated with 4 other functions in a single chip receiver MMIC.

INTRODUCTION

The weight, size and cost reduction is a constant trend in satellite equipments. MMIC allowed an important improvement in the present microwave satellite subsystems for few years. The next step in this way is nowadays the increase of the number of functions on the same MMIC. This trend leads to the size reduction of main microwave monolithic functions and in particular the studied double balanced mixer [1]-[2] which is a key component of Ku band satellite repeaters. More, the coplanar nature of the proposed mixer leads to less expensive chips [3] and allows the use of the Flip-Chip mounting technology, reducing the complete equipment cost. Thanks to its small size, its conversion gain instead of loss and its coplanar technology, the new proposed compact mixer allowed us to design a 14 to 12 GHz single chip MMIC receiver (integrating RF, IF and LO amplifiers and a LO voltage controlled attenuator) for the next generation of telecommunications satellite payloads.
The double balanced coplanar mixer is directly applicable on a standard MMIC process.

MIXER DESIGN

The proposed mixer includes a quad of cold PHEMTs associated with RF and IF 180° active couplers, Fig. 1. The LO coupler is the output of a LO differential amplifier.
The cold PHEMT quad layout has been optimized to reduce its area and to make it more compatible with a coplanar interconnection. The quad is not based on a conventional ring architecture but is in line configuration. The transistors are stacked in parallel like the Gate, Source and Drain electrodes of a FET. The corresponding layout is then more compact but less symmetrical because this topology needs a line to close the two quad extremities. At high frequencies, in particular in Ku band, the electrical length of this line has an important effect. This problem leads us to inject the -RF signal on the center of the quad and 2 split RF signals simultaneously on the 2 extreme Sources of the quad which must be at the same potential.
A particular RF coupler was designed to achieve this special function with 3 outputs. This RF coupler is based on the classical Drain Source 180° active coupler [4]. This well known circuit is very simple but doesn't exhibit very good features (magnitude and phase unbalances). The fundamental problem of this active coupler is that the equivalent electrical circuit of the transistor is not symmetrical between Drain and Source at high frequencies. The principle of the proposed new coupler is to associate 2 active couplers to add the Drain output of the first transistor with the Source output of the second one and reciprocally to add the Source output of the first transistor with the Drain output of the second one. Consequently, the 2 resulting outputs have got the same electrical equivalent circuit and so, are much more balanced than those of a classical Drain Source active coupler. The new architecture needs a third active coupler as first stage to achieve a first 180° split.
The IF combiner is an active circuit too with a common source stage on its 2 inputs followed by an active 180° combiner made with 2 transistors in cascode configuration.

The classical coplanar interconnection items like lines, bends, tees crosses were simulated using COPLAN from ArguMens. The arbitrary geometry coplanar items were simulated using MOMENTUM from Agilent applying a specific method to simulate the coplanar circuits.

RECEIVER DESIGN

The complete single chip MMIC receiver, Fig. 2, includes 5 different microwave functions : the 14 to 12 GHz double balanced mixer associated with a 1 stage RF LNA, a 2 stages IF amplifier, a 4 stages LO differential amplifier and a LO voltage controlled attenuator. The resulting MMIC, Fig. 3, contains 24 PHEMT and is 3.7mm x 4.2mm. The chip, fabricated using the standard 0.2µm PHEMT process of OMMIC foundry, France, was successful at the first pass.

MEASUREMENTS

The mixer RF bandwidth is 12.75 - 14.8 GHz, its LO bandwidth is 1.25 - 3.85 GHz and its IF bandwidth is 10.7 - 12.75 GHz. It provides 2 dB conversion gain. For a -20 dBm LO power, the receiver conversion gain, Fig. 4, can reach 24 dB as a function of the LO variable attenuator. The receiver RF/IF rejection, Fig. 5, is better than -28 dB. Because RF and IF are adjacent bandwidths, the IF amplifier doesn't reject the RF signal. Consequently, the mixer RF/IF isolation can be estimated at about –40dB from the previous complete receiver value decreased by the gain of the RF amplifier and the RF active coupler, more than +10dB. This electrical isolation shows the good balance of the mixer using a compact quad in line configuration. The receiver output power at 1 dB compression gain is always higher than +4 dBm. The output IP3, measured in microstrip test fixture, is about +10 dBm. The receiver LO chain can reach more than 21dB gain, Fig. 6, as a function of the voltage controlled LO attenuator. Table 1 summarizes the main on probe measurement results.

The MMIC receiver was tested on wafer but also in test fixture using a classical microstrip mounting and a Flip-Chip mounting on a coplanar carrier. Fig.7 shows a photograph of the receiver Flip-Chip mounting. This technology is particularly suitable for MMIC having an important number of connections which is typically the case of the studied multifunction receiver. Fig. 8 shows the conversion gain measurement of the Flip-Chip receiver demonstrating the ability of this technology to mount large chips with numerous pads.

CONCLUSION

The use of MMIC allowed an important weight, size and cost reduction of satellite microwave equipments for few years. The next steps are nowadays the integration of an increasing number of functions on the same MMIC, the chip price reduction designing coplanar functions and the use of efficient mounting technology as the Flip-Chip technique. As an answer to these trends, this paper proposes a new compact double balanced coplanar mixer architecture suitable for the satellite repeaters. The mixer is based on a compact PHEMT quad in line configuration directly associated with special RF and IF active couplers. The new mixer area is divided by 3 compared to the present generation currently used in the 14 to 12GHz satellite down-converters. Thanks to its small size, about 1.8mm², and the use of a coplanar technology, the studied mixer was integrated in a single chip MMIC receiver suitable for Flip-Chip mounting, including 5 different functions. This chip measures 3.7mm x 4.2mm and can provide 24 dB conversion gain. The MMIC receiver was successful at the first pass and will be used in the new generation of telecommunications satellite equipments of ALCATEL SPACE INDUSTRIES.

REFERENCES

[1] T.H. Chen and al "Broadband monolithic passive baluns and monolithic double-balanced mixer," *1991 IEEE MTT-S Int Microwave Symp Dig*, pp 861-864, June 1991
[2] JF. Villemazet and al "New compact double balanced monolithic down-converter. Application to a single chip MMIC receiver for satellite equipment," *1998 IEEE MTT-S Int Microwave Dig*, pp 853-856, June 1998
[3] J.A. Eisenberg and al "Slotline and coplanar waveguide team to realize a novel MMIC double balanced mixer," 1992 *Microwave Journal*, pp 123-131, Sept 1992
[4] S.A. Maas “Microwave mixers,” Artech House, 1993

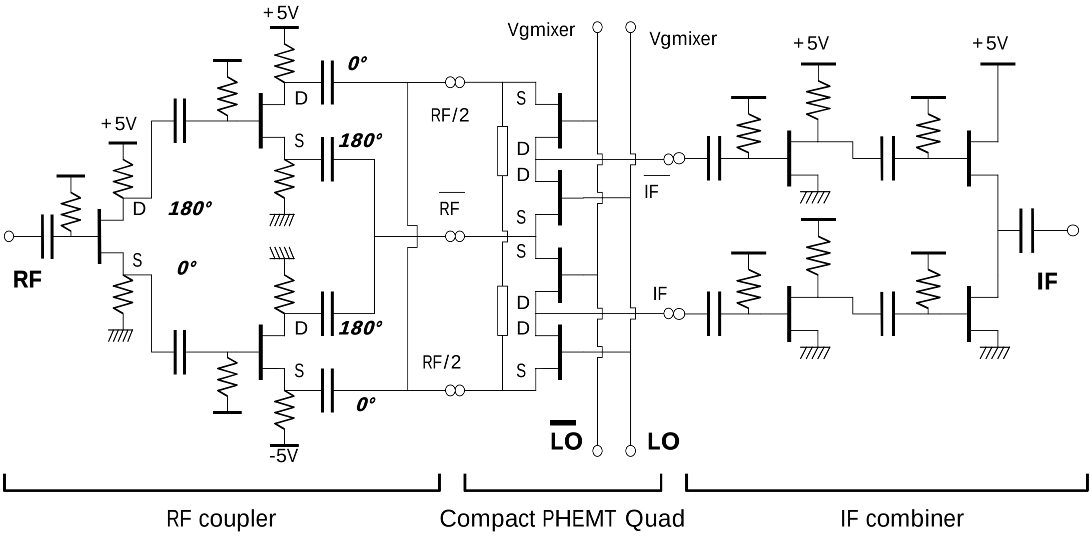

Fig. 1. Proposed compact double balanced mixer schematic

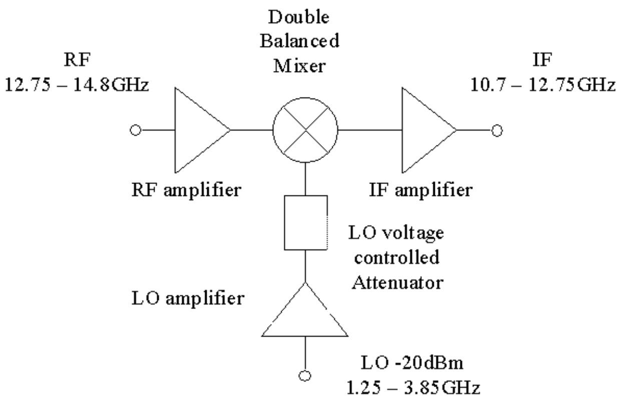

Fig. 2. MMIC receiver architecture

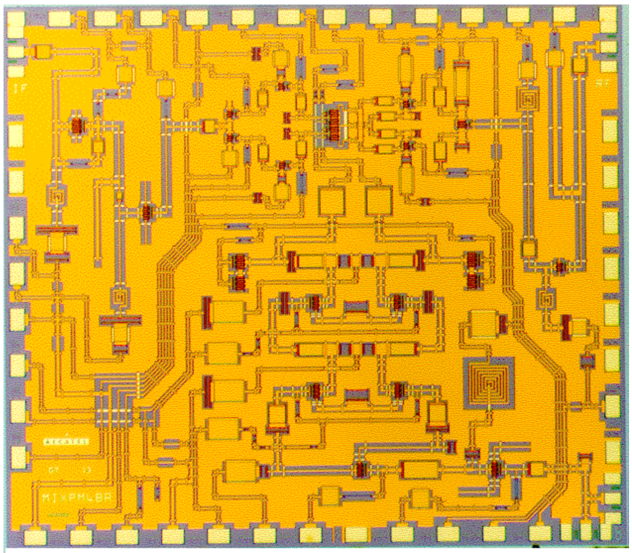

Fig. 3. MMIC receiver - 3.7 x 4.2 mm²

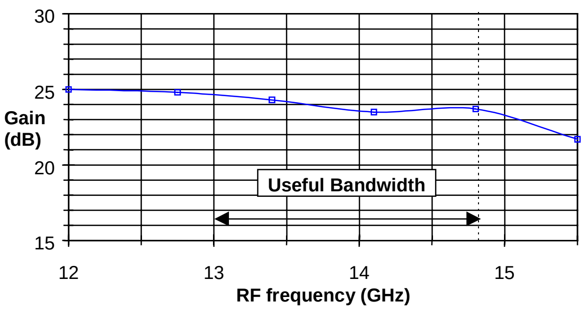

Fig. 4. MMIC receiver conversion gain on-wafer measurement for LO frequency=2.3GHz, LO power= -20dBm, RF power=-30dBm, LO Vatten=-1.5V

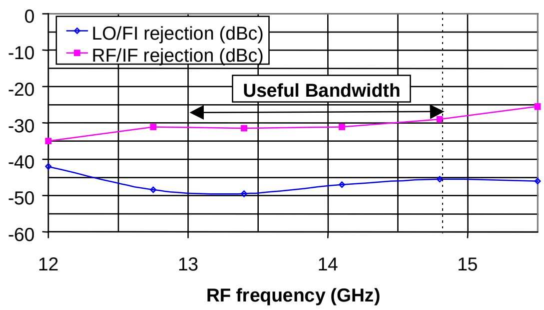

Fig. 5. MMIC receiver output rejections on-wafer measurement for LO frequency=2.3GHz, LO power= -20dBm, RF power=-30dBm, LO Vatten=-1.5V

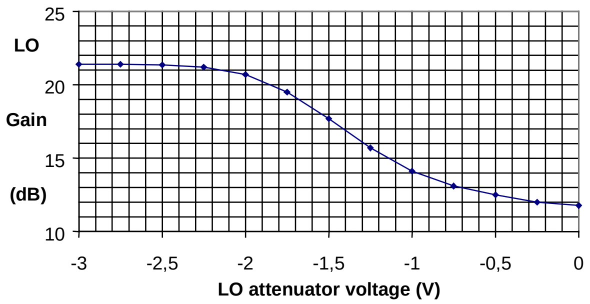

Fig. 6. MMIC receiver LO chain gain on-wafer measurement versus LO attenuator control voltage for a LO frequency=2.3GHz, LO power=-20dBm

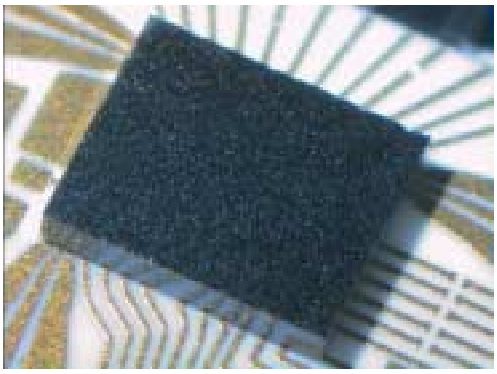

Fig. 7. MMIC receiver Flip Chip mounting

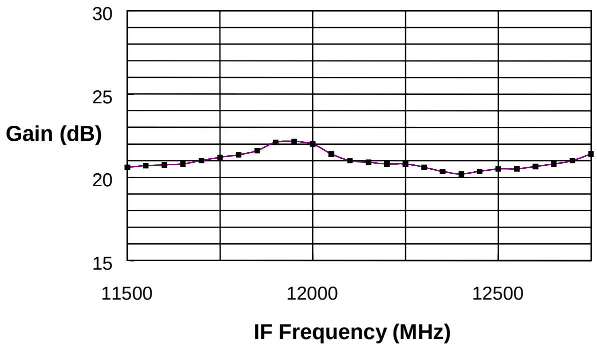

Fig. 8. MMIC receiver conversion gain using a Flip Chip mounting for LO frequency=1.25GHz, LO power= -20dBm, RF power=-30dBm, LO Vatten=-1.5V

Features	**Measurements**
RF frequency	12.75 - 14.8 GHz
IF frequency	10.7 - 12.75 GHz
LO frequency	1.25 - 3.85 GHz
LO input power	-20 dBm
LO gain (50Ω load)	12 dB to 21 dB
Conversion gain	24 dB
P 1dB (PLO = -20 dBm)	+4 dBm
Gain variation vs frequency	< 0.2 dB in 250 MHz
Gain variation vs LO power	< 0.2 dB / dB
Réflexion losses RF port IF port LO port	 < -4 dB < -12 dB < -10 dB
PLO = -20 dBm, PRF = -30 dBm RF / IF Isolation (IF port) LO / RF Rejection (RF port) LO / IF Rejection (IF port)	 < -28 dB < -50 dBc < -45 dBc
Bias supply	-5V, +8V
DC consumption	1.2W
Size	4.2mm x 3.7mm

Table 1 : MMIC receiver on-wafer measurements at 25°C