A MONOLITHIC 5.8 GHZ POWER AMPLIFIER IN A 25 GHZ FT SILICON BIPOLAR TECHNOLOGY

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ABSTRACT

A monolithic integrated radio-frequency power amplifier for the 5.8 GHz band has been realized in a 25 GHz-f_T Si-bipolar production technology (B6HF). The 2-stage push-pull type power amplifier uses a planar on-chip transformer as input-balun and for interstage matching. A high-current cascode stage is used for the driver and for the output stage. At 2.7 V, 3.6 V, and 5 V supply voltage a maximum output power of 21.9 dBm, 24 dBm and 26 dBm at 5.8 GHz is achieved. The small-signal gain is 20 dB.

INTRODUCTION

The push-pull type circuit configuration, invented in the early days of tubes has survived into the semiconductor era with its benefits. There appears a 4:1 load-line impedance benefit for a push-pull combining scheme in an equal-power comparison to a single-ended design. This is an advantageous issue at low supply voltages and at high frequencies. Also the ground connections (bond-wire inductance) are not so critical compared to a single-ended design. However, this approach requires a balun at the output of the power amplifier.
This work presents circuit design and measurement results of an on-chip transformer coupled 2-stage push-pull type amplifier using cascode stages to improve the gain.

CIRCUIT DESIGN

Fig. 1. shows the schematic diagram of the power amplifier. The on-chip transformer X1 acts as balun as well as input matching network. There are several outstanding advantages due to the transformer at the input:

- the input signal can be applied balanced or single-ended if one input terminal is grounded.
- no restrictions to the external DC potential at the input terminals.
- no external input DC blocking capacitor is required.
- relaxed electrostatic sensitive device requirements.

X1 forms a parallel resonant device using two MOS capacitors at the input side connected in anti-series. The turn-ratio of X1 is N = 3:1. The inductance of the primary winding is L_P = 0.8 nH, the inductance of the secondary winding is L_S = 0.5 nH. The total coupling coefficient is k = 0.68. The self-resonant frequency of X1 is 12 GHz.
The driver stage consists of T1 and T2 with 97 μm^2 emitter area each. The DC bias operating current of the driver stage is controlled using the current mirror diode T5 connected to the secondary center tap of the input transformer X1. The driver stage T1, T2 is loaded with a cascode

stage T3, T4 to improve the gain and to avoid the Miller-effect. The cascode stage at the output also improves the robustness against output load-line mismatch. The base voltage of the cascode stage T3, T4 is generated by T6, T7. The interstage power transformer X2 is connected as a parallel resonant device using two anti-series MOS capacitors connected in parallel to the primary winding of X2. The turn ratio of X2 is N = 2:1. Fig. 3 shows the electrical symbol and the winding scheme of the planar transformer. Fig. 4. shows the equivalent circuit of X2. The transformer equivalent model is based on [1]. The inductance of the primary winding is L_P = 0.88 nH, the inductance of the secondary winding is L_S = 0.33 nH. The total coupling coefficient is k = 0.46. The self-resonant frequency of X2 is 8.5 GHz.
The output stage is very similar to the input stage, except that the effective emitter area of T8 to T10 is 290 μm^2. The most critical challenge in this design is to achieve a smooth and steady bias voltage at the bases of the cascode stages T3, T4 and T10, T11.

EXPERIMENTAL RESULTS

Fig. 2. shows the chip photograph of the power amplifier. The chip size is 1.56 x 1 mm^2. The chip is fabricated in a standard 25 GHz-f_T, 0.8 µm, 3-layer-interconnect silicon bipolar production technology of Infineon B6HF [2]. The collector-base breakdown voltage is BV_{CB0} = 18 V and the collector-emitter breakdown voltage is BV_{CE0} = 3.9 V.
Fig. 5. shows the schematic diagram of the power amplifier test-board. The input of the amplifier is connected via a 50 Ω micro-strip line to the input signal. Two additional external chip capacitors are bonded to the cascode stage of the driver and output stage each. The balanced output is connected via 50 Ω micro-strip lines to the SMA connectors. The supply voltage is connected using λ/4-transformers. Each output of the test-board is connected to two slide-screw tuner to adjust the optimum load impedance. Fig. 6. shows the photograph of the test board. The chip is bonded on a Rogers RO4003 substrate.
Fig. 7. shows the output power versus frequency at Pin = 10 dBm. The power amplifier is operating in a pulsed mode with a duty cycle of 12.5 %. The pulse width is 0.577 ms. The maximum output power is 26 dBm at 5.8 GHz and 5 V. The bandwidth is limited by the characteristic of the slide-screw tuner around the optimum load impedance, not by the amplifier. The maximum PAE is 13 % at 5.8 GHz and 3.6 V. Fig. 8. Shows the output spectrum at Pin = 10 dBm and 5 V. Tab. 1. shows the performance summary. To increase the relatively poor PAE and the amplifier stability, the cascode bias reference network has to be improved.

CONCLUSION

We have presented an integrated 5.8 GHz power amplifier in a 25 GHz f_T Si-bipolar technology. The circuit design is based on a 2-stage push-pull type amplifier using on-chip transformer coupling for input and interstage matching. A high-current cascode stage is used in the driver and output stage to increase the gain. The maximum output power is 21.9 dBm, 24 dBm and 26 dBm at 2.7 V, 3.6 V and 5 V supply voltage and 5.8 GHz. The most critical challenge is to achieve a smooth and steady bias operating point of the high-current cascode stages.

REFERENCES

[1] Kehrer, D. *et al.*, "Modeling of Monolithic Lumped Planar Transformers up to 20 GHz," in *IEEE Custom Integrated Circuits Conference 2001,* San Diego, IEEE, May 2001.

[2] Klose, H. *et al.*, "B6HF: A 0.8 Micron 25 GHz / 25 ps Bipolar Technology for Mobile Radio and Ultra Fast Data Link IC Products," in *IEEE Bipolar Circuits and Technology Meeting*, pp. 125-127, IEEE, 1993.

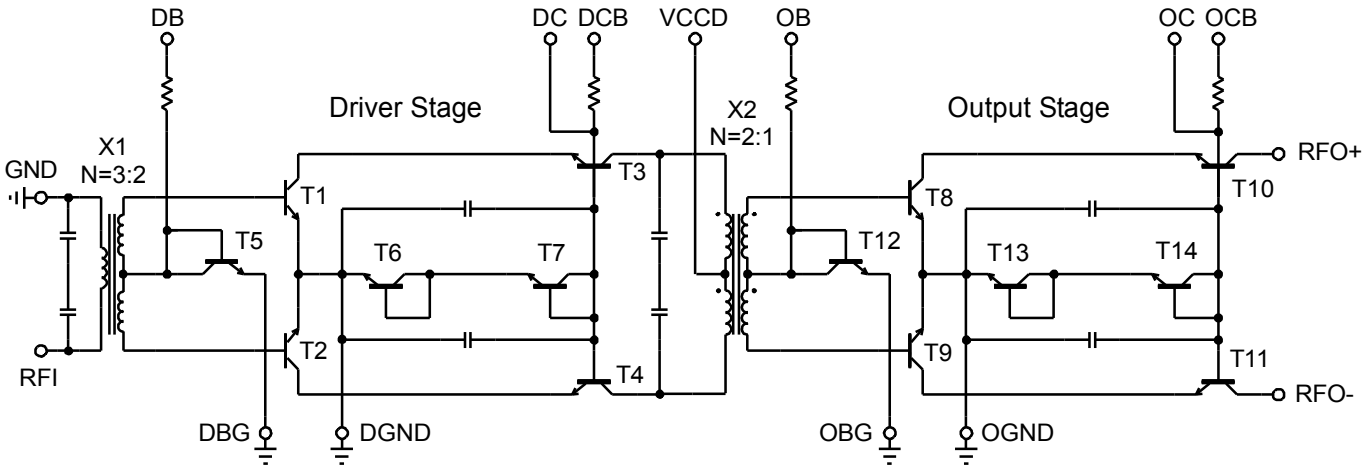

Fig. 1. Schematic diagram of the 5.8 GHz Si-bipolar power amplifier

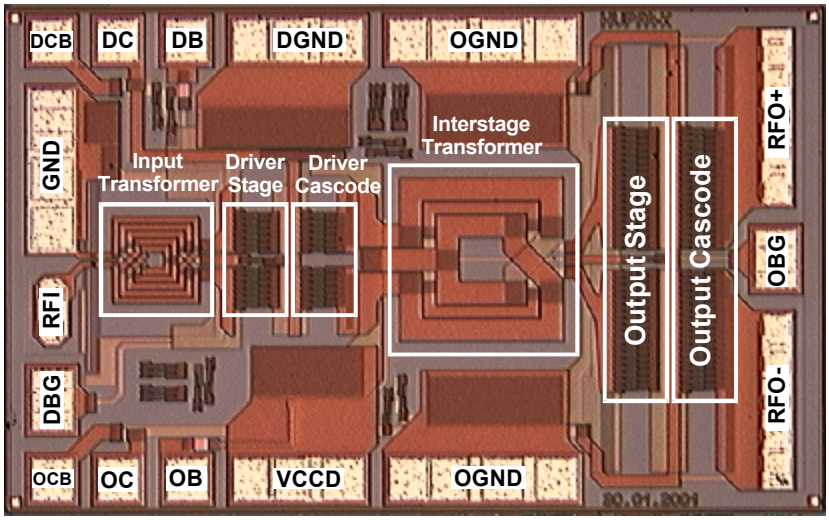

Fig. 2. Chip photograph (size: 1.56 x 1 mm^2)

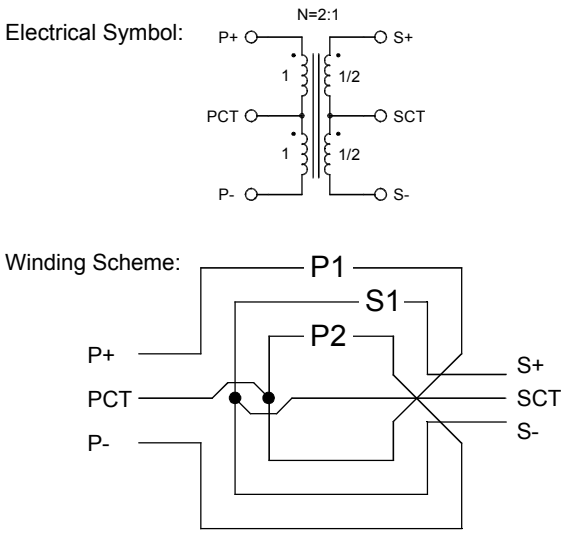

Fig. 3. Electrical symbol and winding scheme of the on-chip transformer X2 (N=2:1)

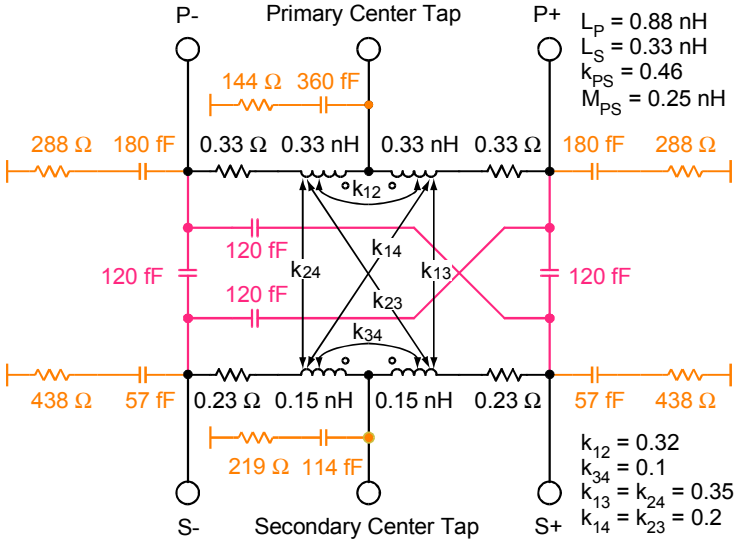

Fig. 4. Equivalent model of the on-chip transformer X2 (N=2:1)

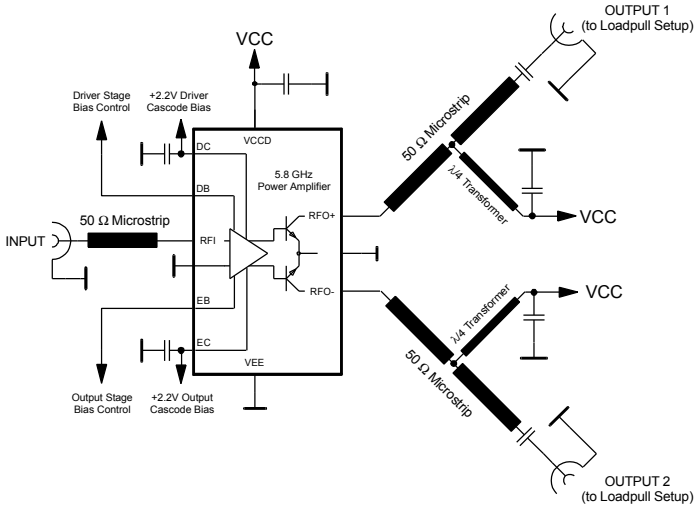

Fig. 5. Power amplifier test-board schematic diagram

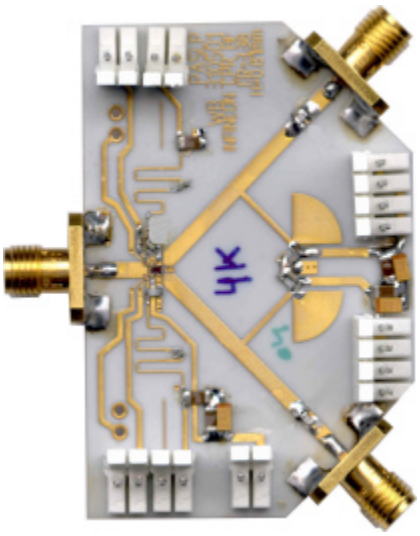

Fig. 6. Photograph of the power amplifier test-board

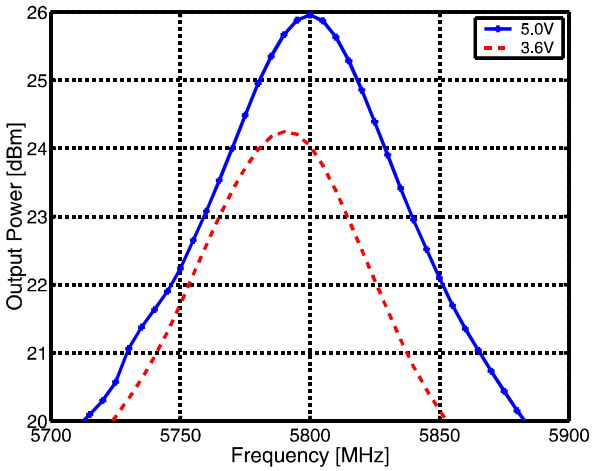

Fig. 7. Output power versus frequency (Pin = 10 dBm, f = 5.8 GHz).

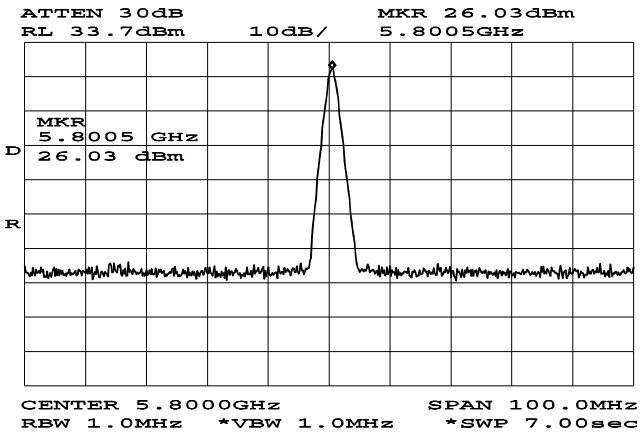

Fig. 8. Output spectrum (Pin = 10 dBm, f = 5.8 GHz, VCC = 5 V).

Supply Voltage Range	2.7 – 5 V		
Small-Signal Gain (f = 5.8 GHz)	20 dB		
Input VSWR (Pin = 10 dBm, f = 5.8GHz)	2.2		
Chip Size	1.56 x 1 mm^2		
Technology	Si Bipolar 0.8 µm, 25 GHz f_T (B6HF)		
	VCC = 2.7 V	VCC = 3.6 V	VCC = 5 V
Output Power (Pin = 10 dBm, f = 5.8 GHz)	21.9 dBm	24 dBm	26 dBm
PAE (Pin = 10 dBm, f = 5.8 GHz)	11 %	13 %	12 %

Tab.1. Performance Summary (T = 300 K, 12.5 % duty cycle, 0.557 ms pulse width).