LATEST ADVANCES IN HIGH POWER SI MMIC

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Abstract:

During the past years Si MMIC have entered the cellular base station arena. It has been necessary to demonstrate the technical capabilities of these products , in terms of power and in terms of bandwidth/gain flatness. These two particular topics are essential in this multiband high power domain , where linearisation is very often required. This article presents the technical difficulties specific to high power Si MMIC, the associated solutions, and two circuits demonstrating their power and bandwidth capabilities .

I.TECHNICAL PROBLEMS

Power performance:

Several combined problems vorbid the design of multistage power amplifiers, in Si MMIC format, by using a classical approach, such as described in fig 1, where cascaded single ended transistors are lined-up:

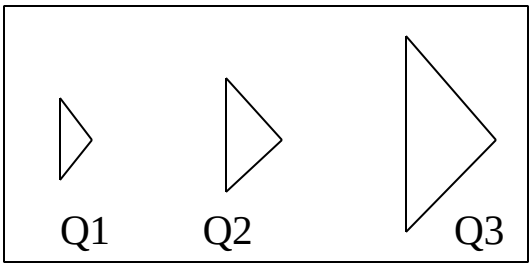

fig 1:classical multistage PA architecture.

The output transistor is very large, because of the power requirements (several tens of watts), and therefore features three characteristics:
-sub-ohm input and output impedances in the gate and drain plane.
-physical size much larger than the passives (around 20X).
-very large scaling factor compared to models fet size.

The inductances and transmission lines are very lossy (Quality factors around 5 in the 1-2 GHz band). The losses result from coupling by proximity from the metal to the substrate. Their physical size is much lower than the transistors (already mentionned earlier).

The classical approach described earlier, combined with these active and passive elements results in :
-very high losses in the matching networks due to low impedances and low Qs.
-significant phase shift at excitation and recombination of the different fingers due to the large ratio between active and passive physical size, therefore power loss.
-inaccurate simulation because of the excessive scaling factor.
-potential thermal problems.

Bandwidth / gain flatness performance :

In multistage power amplifier design, the in band gain ripple performance is more or less proportional to the amplifier's bandwidth's inverse. In other words the broader the amplifier, the flatter the gain versus frequency.
Let's then consider what the bandwidth limiting factors are:

-impedance transformation ratio
-Q factor
-matching networks topology.

The first one is applicable to the input and output matching networks , where the bandwidth limiting effects are at worst , but also to the interstage matching networks. The impedance transformation ratio at the output is mainly related to the desired output power and then worsens with power.

The Q factor is more or less technology related and is a direct translation of the parasitic capacitances of a given transistor technology. Its peak effect occurs in the matching of the gate or base side of the input stage to 50 ohms.

II.SOLUTIONS

Power solution[1]:

Two major techniques cancel most of the effects described above. The first one is the use of size limited transistors and the second one their combination in a branch structure amplifier. The former allows accurate simulations because of reasonnable scaling factor with respect to models, the matching loss becomes acceptable due to higher impedances, and finally a good in phase excitation / recombination is obtained between fingers because of the comparable size between passives and actives. The latter allows the obtention of the required output power levels. It is to be noted that the phasing problem between fingers can be further optimised by the extension of the unit finger width, which reduces the number of fingers.
In addition the thermal resistance is improved because of the heat source spreading.

Bandwidth / Gain flatness solution[2] :

Four combined techniques circumvent the problem:

-Use of limited gate periphery transistors, which increases the impedance level at the device terminals.
-Minimize the transistor size ratio between stages.
-Use of shunt inductance right in the device plane , in order to "move" the capacitive impedance of the transistor to the Smith chart real axis, and aiming at the chart center.

The first technique limits the power capability, and then reaching superior power levels requires paralleling or combining. Conventional combiners being too lossy in Silicon form, other combining techniques have to be used .This leads to the fourth following technique :

-combining /paralleling line-ups at impedance level as close to 50 ohms as possible.

In addition to the bandwidth /gain flatness feature, these techniques provide the very same advantages than the power solution described above.

III.SOLUTIONS VALIDATION

A 3 stages 30W GSM amplifier using the power solution has been designed and tested.

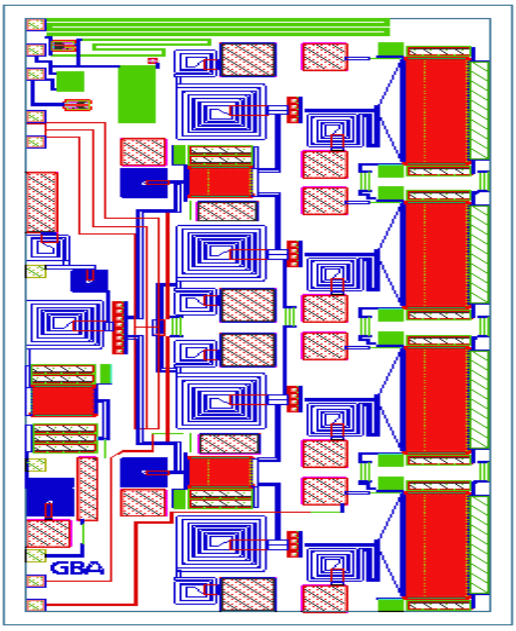

Fig 2 : 30W GSM amplifier layout

The figures 3,4 and 5, and table 1 present the performances of the circuit.

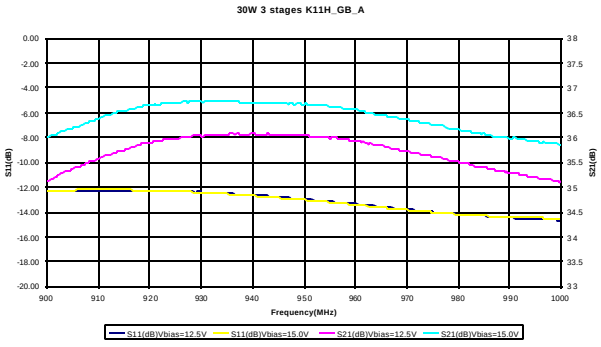

Fig 3 : frequency sweeps @ P1dB and in small signal

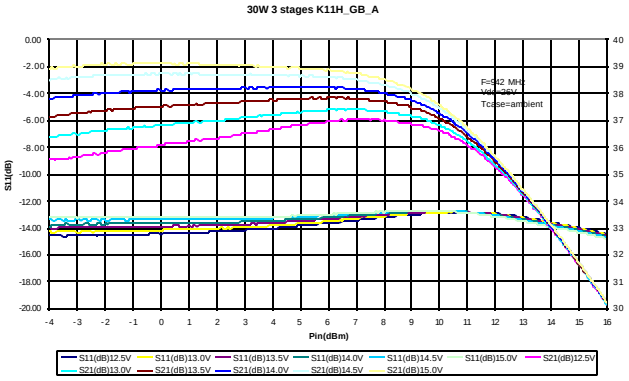

Fig 4 : Gain & S11 power sweeps @ 942 MHz

P1dB(dBm)=45.1
PAE(%)=50.5
S11(dB)=-14
Gain(dB)=36.0

Table 1 : large signal performances @ 942 MHz

A 20W WCDMA power amplifier with very low gain ripple has been designed, using the bandwidth / flat gain ripple technique.
The MMIC topology is described in fig 5.

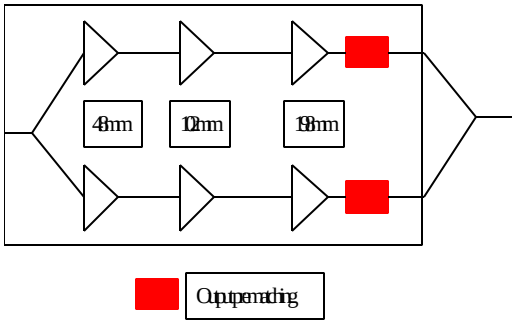

Figure 5 : MMIC topology.

The device layout is shown in fig 6.

The large signal gain and S11 are shown in fig 7 and fig 8.

The PAE (%) and the gain(dB) versus output power are given in fig 9 .

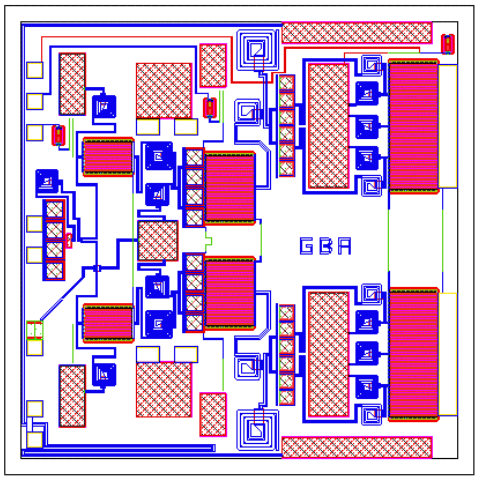

Fig 6 : device layout.

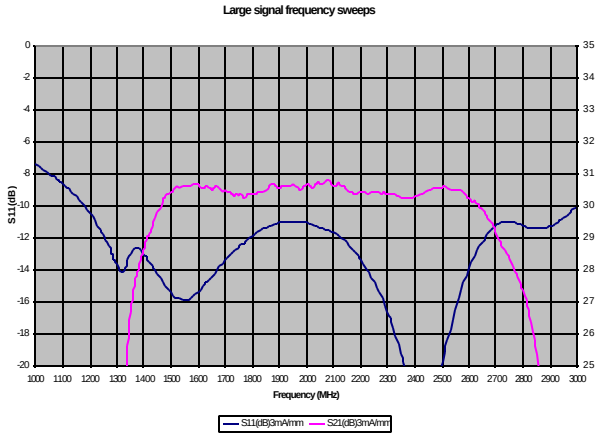

Fig 7: broadband large signal gain(dB) & S11

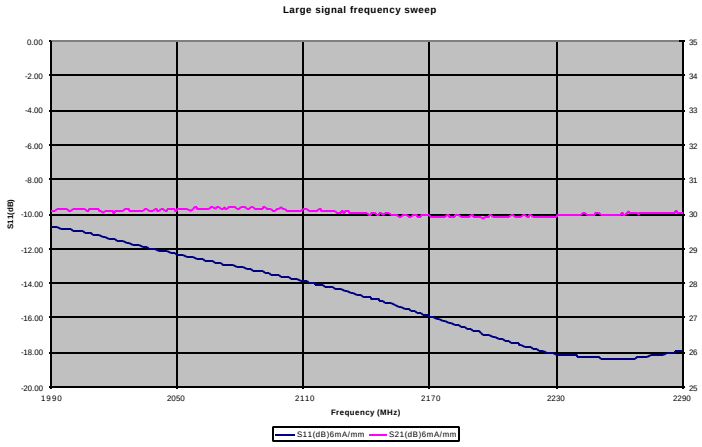

Fig 8: large signal gain(dB) and S11(dB) in 5X the UMTS bandwidth.

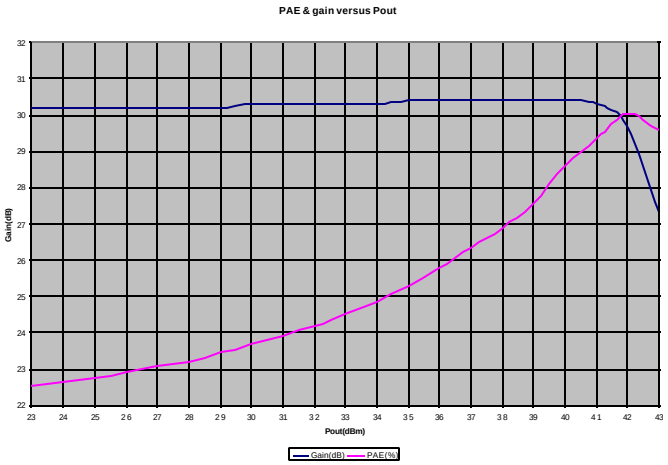

Fig 9 : Gain(dB) and PAE(%) versus Pout(dBm).

IV.CONCLUSION

This article has presented the intrinsic problems to high power silicon MMIC amplifiers, such as very poor quality passives, very large reflection coefficient transistors , and their respective incompatibility . Two solutions have been proposed, aiming at resolving the power problem and the bandwidth / gain flatness issue. One validation per solution was shown , a 30W 900 MHz 3 stages MMIC , and a very broadband 20W WCDMA 3 stages MMIC featuring 57% relative bandwidth and 0.2dB gain ripple .

REFERENCES

[1] G.Bouisse " High power Silicon MMIC design for wireless base stations." IEEE Eumw symposium 2000.
[2] G.Bouisse "0.2db gain ripple-20W-WCDMA Si MMIC ".IEEE EuMC-ECWT symposium 2001