2^7-1 SiGe PRBS Generator IC up to 86 Gbit/s

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Abstract— **Design and performance of a high speed 2^7-1 pseudo random bit sequence (PRBS) generator chip is presented. The circuit operates at a speed up to 86 Gbit/s and is fabricated in an advanced SiGe technology with a cutoff frequency f_t of 200 GHz and a maximum oscillation frequency f_{max} of 240 GHz. It is based on a multiplexed linear feedback shift register and has a power consumption of 950 mW. An 1:2 demultiplexer, made in the same technology for up to 86 Gbit/s is also presented. With this two circuits electrical data transmission up 86 Gbit/s is demonstrated.**

I. INTRODUCTION

For testing high-speed components such as multiplexers, demultiplexers and flip-flops pseudo random bit sequences are used (PRBS). Also for characterizing large signal behavior of analog devices like linear and limiting amplifiers PRBS generators are needed. With such a generator eye diagrams can be measured and jitter and rise/fall time can be determined. But commercial instrumentation for PRBS generation is limited to 48 Gbit/s and is very expensive. Another point is, that this instrumentation is in big boxes, which can't be moved close to the DUT especially for on-wafer testing. At 40 Gbit/s and above, cable loss is becoming a dominating factor. In many on-wafer measurement setups the speed and the bandwidth is limited by the used cables and probes and lower than the speed of the DUT, especially when it is made in an advanced technology.

The present work introduces a high speed 2^7-1 PRBS generator IC. It is implemented in a half rate architecture and needs only one half rate clock signal and a reset signal to start the generator. So it is very easy to use, needs no external electrical components and can be packaged in a small box. This box can be placed very close to the DUT, avoiding loss of long cables. For on-wafer measurements it would also be possible to integrate this circuit in a kind of active probe.

Since no bit error tester for such high data rates are available, an 1:2 demultiplexer was designed. So the data stream can be transferred to a lower bit rate and the bit error rate can be measured with a commercial bit error rate detector.

A. Comparison to previous publications

High speed PRBS generator ICs use shift registers at lower speed and generate the high speed signal using multiplexing techniques. In [1] the shift registers operate at the quarter speed and in [2]-[4] at the half speed of the output data rate, similar to this work. Fig. 1 shows the bit rate versus power consumption of the fastest PRBS generator ICs published so far compared to this work. It clearly indicates the tremendous increase in speed, which is nearly doubled. The power consumption of 950 mW is smaller than in all other publication, but it has to be considered that [1], [2] and [4] have a pattern trigger implemented into the chip.
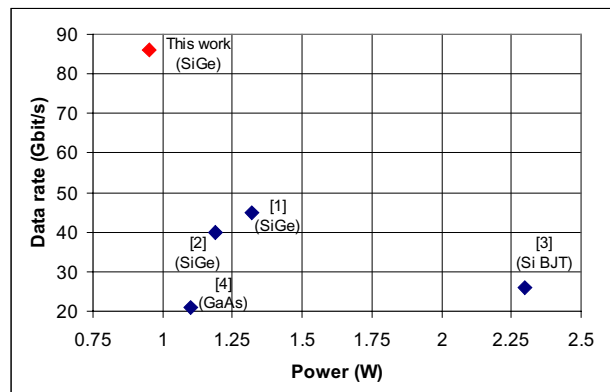

Fig. 1: Comparison of PRBS generator IC performance.

II. CIRCUIT DESIGN

The circuit is based on a multiplexed linear feedback shift register similar to [4]. Fig. 2 shows the block diagram of the PRBS generator IC. The two loops of the shift registers use seven latches. The output of each loop is multiplexed to the PRBS output data stream at a bit rate which is twice of the clock frequency. Because the latches operate at only half of the speed, the design of the latches, the clock-tree and the clock buffers is less critical and power can be saved.

In the shift registers the XOR function has to be calculated and fed into the first latch. In order to increase the time for this calculation, the clock is applied to the latches in the opposite way to the data stream. Because of the line length the first latch after the XOR gets the clock about 3 ps later. Also the timing for the multiplexer is very critical. Other publications are using a different clock for the multiplexer to adjust the timing [2, 4]. The goal was to have a chip which is easy to use and can operate with only one clock signal. So the last latch was modified with an additional fast data output, so that the multiplexer could be applied with the same clock. An additional advantage when the circuit operates with only one clock signal is, that the frequency can be increased or decreased without new clock alignment. So when using this circuit in measurements the data rate can be changed very easily. At the power up of the circuit all latches could have the
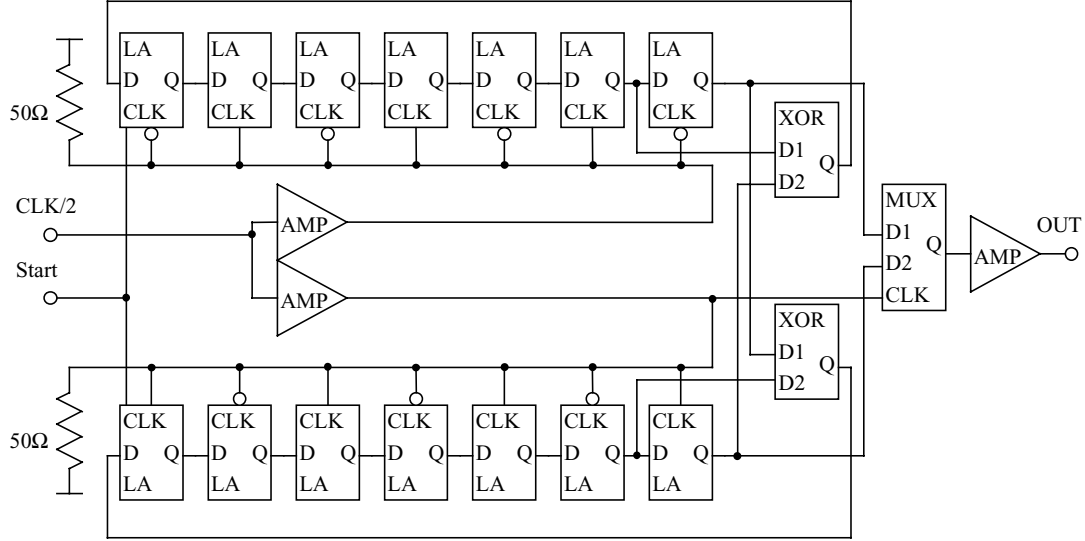
Fig. 2: Principle of the PRBS generator IC.

zero state. So a starter is applied to the first latch to feed it with ones to start the bit sequence.

A. Technology

The progress of the newest SiGe technologies allow to integrate such an IC in SiGe [5, 6]. The advantage of this technology is, that it has a higher yield and more matallization layer for the extensive wiring are available compared to the most III-V technologies.

The circuit was fabricated in the advanced SiGe process from Infineon, which has a cutoff frequency f_t of 200 GHz and a maximum oscillation frequency f_{max} of 240 GHz. The circuit is implemented in emitter coupled logic (ECL) and takes a current of 220 mA at –4.3 V (P = 950 mW). At lower speed the current of the latches can be reduced. For 40 Gbit/s the power consumption can be lowered to 500 mW by reduction of the power supply voltage. Fig. 3 shows a picture of this chip with a chip size of 1.2 x 1.6 mm^2.
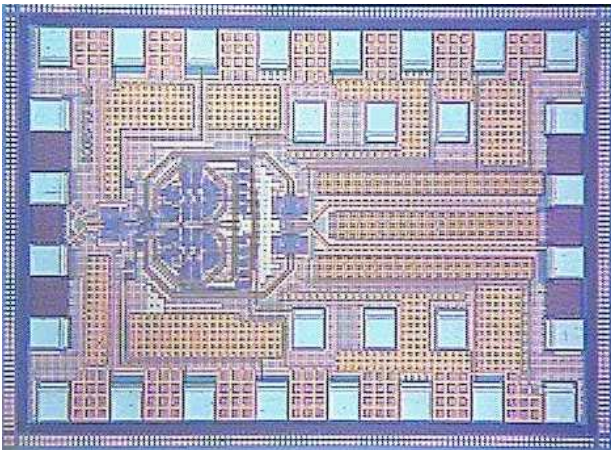
III. RESULTS

For measurements the chip is mounted in a Rogers board with a cutout and connected with ribon bonds to grounded coplanar lines for the clock input and the high speed data output. To avoid additional cables and adapters, semirigid cables were directly attached to the Rogers board. This is an easy and cheap mounting technique and allows very short cables for the measurement.

For testing only the clock has to be applied and the output is measured with an oscilloscope (86110B from Agilent with the 65 GHz sampling unit 86116A and the precision tame base unit 86107A). Fig. 4 and 5 show the differential measured eye diagrams at 40 and 86 Gbit/s. For 40 Gbit/s a very nice and clean eye diagram is measured with an amplitude of 500 mV$_{pp}$ and the rise time (20-80%) is about 8 ps. A very small RMS-jitter of 360 fs and peak-to-peak jitter of less than 2 ps was measured. Note that the jitter of the oscilloscope is included in this measurement.

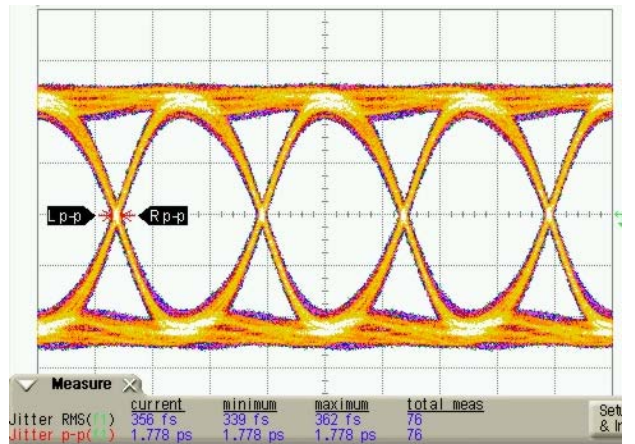Fig. 3: Picture of the fabricated IC, chip size 1.2 x 1.6 mm^2.

Fig. 4: Differential measured eye diagram of the output of the PRBS generator IC at 40 Gbit/s, scale: 100 mV/div, 10 ps/div.
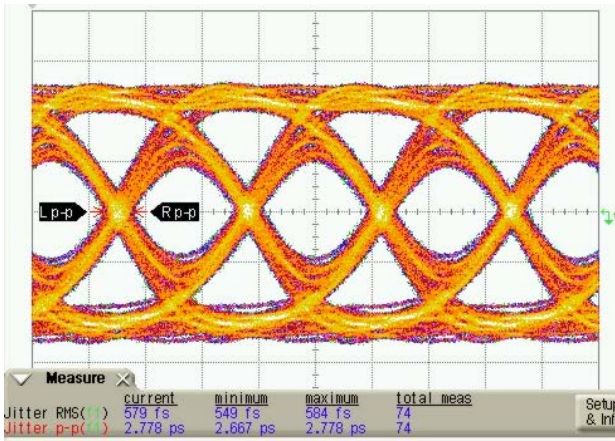
Fig. 5: Differential measured eye diagram of the output of the PRBS generator IC at 86 Gbit/s, scale: 100 mV/div, 5 ps/div.

At 86 Gbit/s the eye opening is getting smaller. But this is not surprising when the bandwidth of the oscilloscope, the cables, the phase shifters to enable differential measurement and the mounting with bond wires are considered. The limited bandwidth of the output buffer also accounts for the smaller eye opening, but this is expected to have a minor influence than the points mentioned before. The RMS jitter is with 580 fs still very small.

To check if the shift registers are working properly and generating a correct pattern, additional dividers were used to get a pattern trigger. With this trigger the bit pattern can be measured. Fig. 6 and 7 show the differential measured bit pattern at 40 and 86 Gbit/s. Because the pattern is stable, the shift registers are working properly. Also this measurement indicates the bandwidth limitations of the measurement setup, as mentioned above. The single bits at 86 Gbit/s are not reaching the rails.
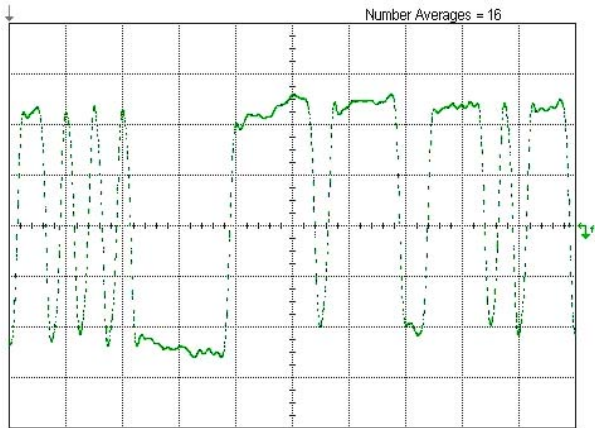

Fig. 6: Differential measured bit pattern at 40 Gbit/s, scale: 100 mV/div, 100 ps/div.
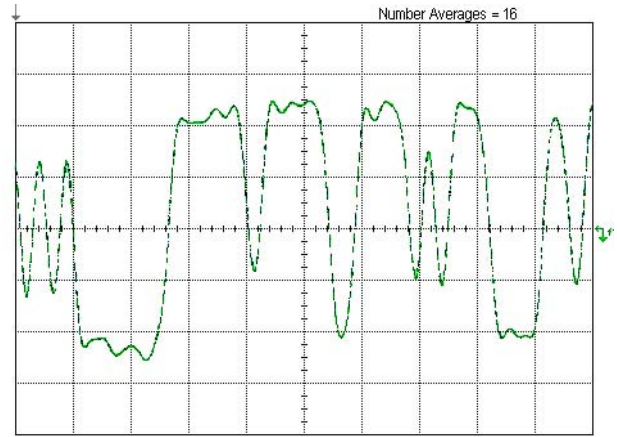

Fig. 7: Differential measured bit pattern at 86 Gbit/s, scale: 100 mV/div, 50 ps/div

IV. DATA TRANSMISSION AT 80 AND 86 GBIT/S

A high speed 1:2 demultiplexer was also designed and fabricated on the same wafer as the PRBS generator IC. It is a straight forward design with two flipflops for sampling the corresponding bits, data input and output amplifiers and a clock buffer. At one output an additional latch is used, so that both data outputs have the same phase. It is implemented in ECL and the power consumption is 1025 mW. Also this circuit is mounted on a Rogers board attached with semirigid cables as the PRBS generator IC.

For realizing electrical data transmission at 80 and 86 Gbit/s the demultiplexer was put after the PRBS-generator chip as it is shown in fig. 8.
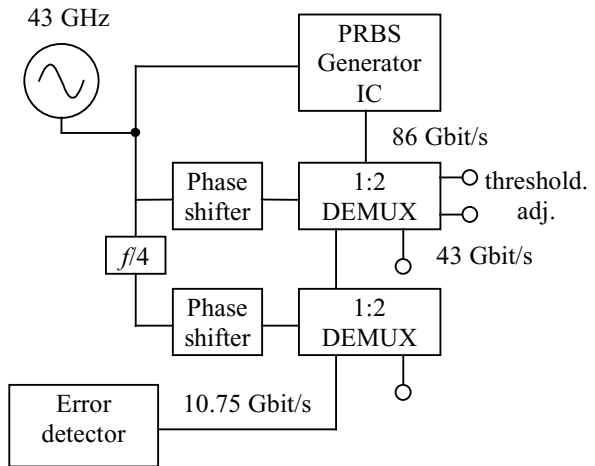

Fig. 8: Block diagram of the measurement setup for 86 Gbit/s data transmission.

The PRBS generator IC produces the 86 Gbit/s data stream which is applied to the high speed 1:2 demultiplexer. Both chips are driven with the same 43 GHz clock, whereas the clock for the demultiplexer can be adjusted with a phase shifter. One of the 43 Gbit/s outputs of the demultiplexer is connected to an additional 1:2 demultiplexer. The 43 GHz clock is divided by four to drive this second demultiplexer. So this demultiplexer is used as a flipflop to get each forth bit to the output. Fi-

nally the signal is down converted to 10.75 Gbit/s, so a commercial 10 Gbit/s error detector could be used. With this setup error free data transmission up to 86 Gbit/s could be achieved, independent which output of the first demultiplexer is used.

With adjusting the threshold at the offset pins and the phase of the first 1:2 demultiplexer the vertical and horizontal eye opening can be measured. This measurement has been done with several attenuators at 80 and 86 Gbit/s. The result of these measurements are shown in fig. 9 for the horizontal and fig. 10 for the vertical eye opening. For the limit in all measurements a bit error rate of 10^{-9} was used. The figures on the right side of the plots indicate the used attenuator for the measurement.
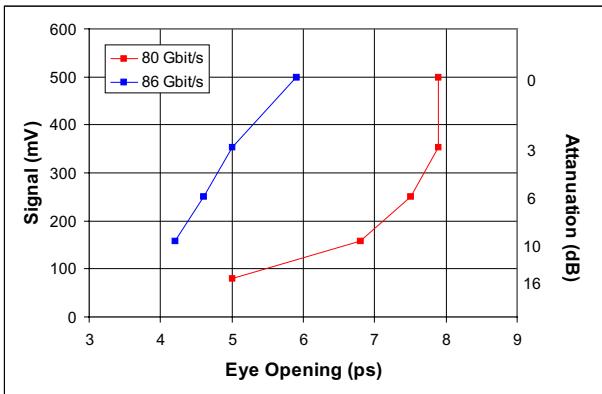

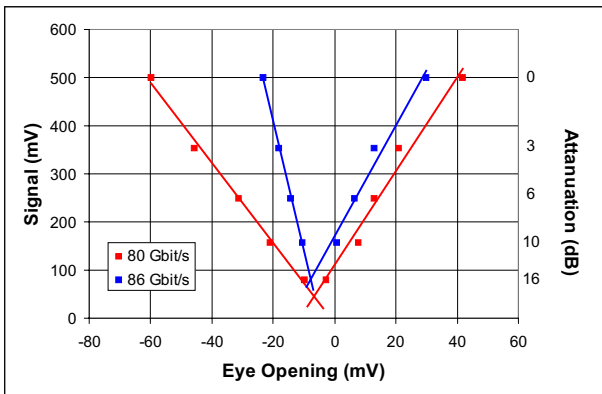Fig. 9: Measurement of the horizontal eye opening at 80 and 86 Gbit/s at a bit error rate of 10^{-9}.

Fig. 10: Measurement of the vertical eye opening at 80 and 86 Gbit/s at a bit error rat of 10^{-9}.

The adjustment of the measurement setup at this high speed data transmission is very critical. For example an offset of the applied clock, unbalanced behavior of the circuit or unsymmetry in the mounting can lead to two different eye openings. So always at least two eye openings were measured. If there was only a small difference the results are averaged otherwise the setup was readjusted. This also reduces the errors, caused form phase changes through temperature drift from cables and circuits or movements from the setup by changing the phase of the manual phase shifters.

The measurements show a horizontal eye opening of 5.9 ps at 86 Gbit/s (7.9 ps at 80 Gbit/s). With adding attenuators in the data path, the phase margin is becoming smaller. At 86 Gbit/s 10 dB (at 80 Gbit/s 16dB) attenuation could be added and still error free data transmission could be achieved. In the vertical direction an eye opening of 53 mV at 86 Gbit (101 mV at 80 Gbit) could be measured. When adding attenuators the eye opening is becoming smaller. Extrapolating this points of the measurements result in the sensitivity of the transmission. At 86 Gbit/s the sensitivity is at 50 mV and at 80 Gbit/s 100 mV. With this measurement the PRBS generator IC and the 1:2 demultiplexer are verified up to 86 Gbit/s.

V. CONCLUSION

We have presented a broadband 2^7-1 PRBS generator IC and an 1:2 demultiplexer fabricated in an advanced SiGe bipolar technology. The generator operates up to a data rate of 86 Gbit/s with a power consumption of 950 mW. To our knowledge is this the highest data rate of an PRBS generator IC reported to date. With this two circuits we could build up electrical data transmission at 86 Gbit/s and verify so the two ICs.

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